User's Manual

HIGH SPEED COUNTER MODULE

(AD61)

A Series Programmable Controllers

MITSUBISHI

Cat. No. UMHS

INTRODUCTION

Thank you for your purchase of Mitsubishi General-Purpose Programmable Controller MELSEC-A. Prior to use, please read this User's Manual carefully to fully understand the functions and performances of the A series programmable controller and also to use it correctly.
Please forward this User's Manual to the end user.

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1. GENERAL DESCRIPTION

This manual describes the AD61 and AD61S1 high speed counter modules giving handling instructions and basic programming information. The AD61S1 allows counting pulses of long rise and fall times (more than 50μsec). (Unless otherwise specified, the AD61 and AD61S1 are referred to as "AD61".)
The AD61 high speed counter module is used in conjunction with MELSEC-A series programmable controllers.

The following manuals may also be required:

A CPU User's Manual
A CPU Programming Manual
A CPU Data Link User's Manual

POINT

In this manual, I/O signals to and from the programmable controller CPU are explained on the assumption that AD61 is loaded in No. 1 slot of the main base unless otherwise specified (except circuit example in the Appendix).

2. SYSTEM CONFIGURATION

2.1 General Description of System

A configuration example of an independent system is shown below. For the use of the AD61 in a data link system, refer to Section 2.2 "Applicable System."

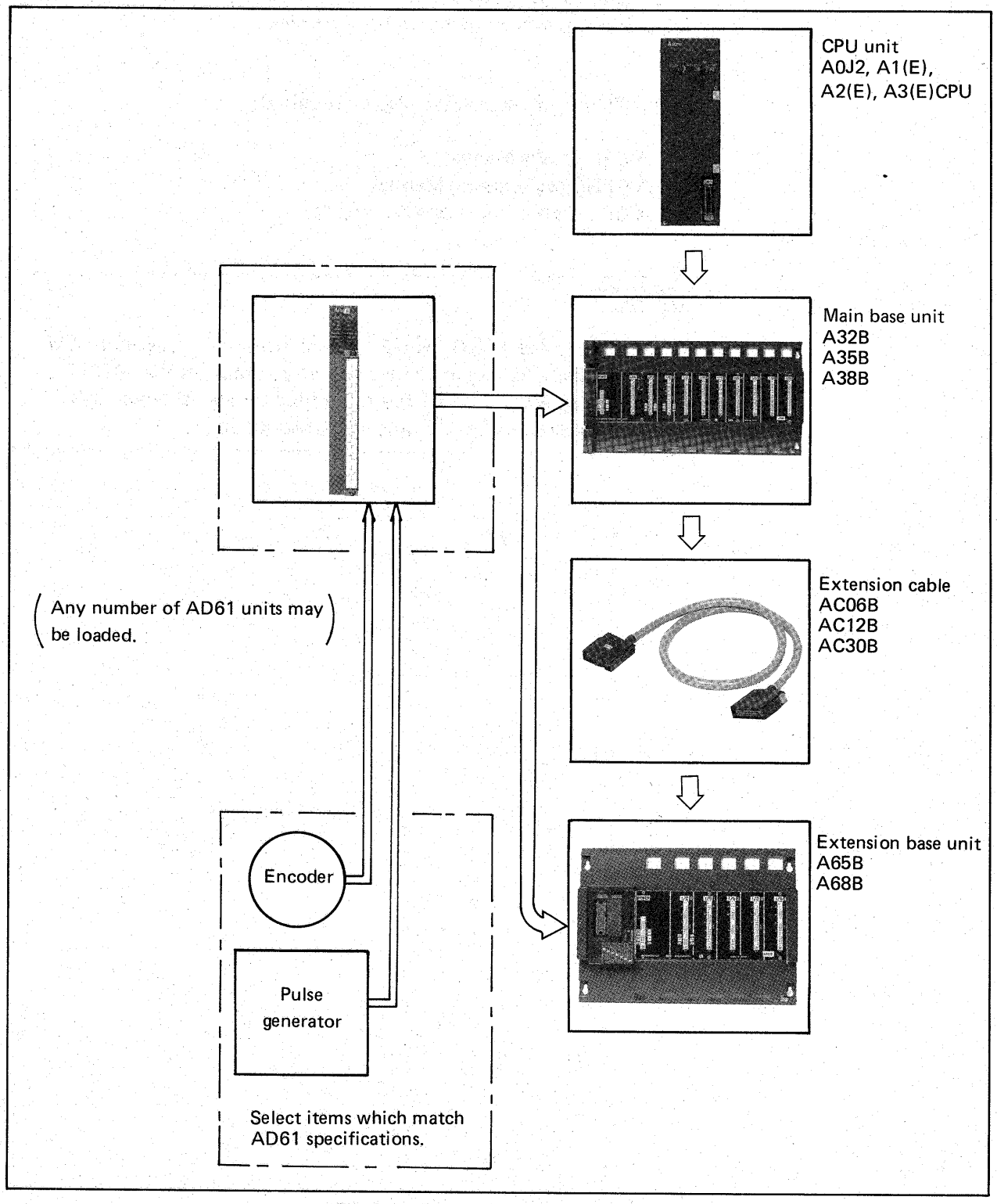


Fig. 2.1 Overall Configuration Diagram

2.2 Applicable System

(1) AD61 can be used with the following CPUs:

Applicable models	A0J2CPU A1(E)CPU A2(E)CPU A3(E)CPU

(2) The AD61 can be loaded into any slot of a base unit with the exceptions given below:

- If the AD61 is loaded into an extension base unit without a power supply unit, care must be taken to ensure that the power capacity is sufficient.
  (For the selection of power supply unit and extension cable, refer to Section 3.4 to 3.5 of the CPU User's Manual)

- For a data link system, the CPU must be of one of the following types.

A1(E)CPU P21/R21 A2(E)CPU P21/R21 A3(E)CPU P21/R21

2.3 Cautions for System Configuration

Take special care of the following points.
When the PC power is turned on or off, process output may not perform normal operation temporarily due to the difference between the delay time and rise time of the power of PC mainframe and the external power (especially DC) at the outputs. Also, in the event of external power supply failure or PC failure, the output process may perform abnormally.
In order to prevent the aforementioned abnormal operations and also from a failsafe viewpoint, program in precautions (such as an emergency stop circuit, a protection circuit, and an interlock circuit), against any abnormal operation which may lead to machine damage. The following page shows an example of such precautions.

3. SPECIFICATIONS

This chapter describes the general specifications and performance specifications of the AD61.

3.1 General Specifications

The general specifications of AD61 are shown in Table 3.1.

<table>
<tr><th>Item</th><th colspan="5">Specifications</th></tr>
<tr><td>Operating ambient temperature</td><td colspan="5">0 to 55°C</td></tr>
<tr><td>Storage ambient temperature</td><td colspan="5">−10 to 75°C</td></tr>
<tr><td>Operating ambient humidity</td><td colspan="5">10 to 90%RH, no condensation</td></tr>
<tr><td>Storage ambient humidity</td><td colspan="5">10 to 90%RH, no condensation</td></tr>
<tr><td rowspan="3">Vibration resistance</td><td rowspan="3">Conforms to JIS C 0911</td><td>Frequency</td><td>Acceleration</td><td>Amplitude</td><td>Sweep Count</td></tr>
<tr><td>10 to 55Hz</td><td>−</td><td>0.075mm</td><td rowspan="2">10 times
*(1 octave/minute)</td></tr>
<tr><td>55 to 150Hz</td><td>1g</td><td>−</td></tr>
<tr><td>Shock resistance</td><td colspan="5">Conforms to JIS C 0912 (10g x 3 times in 3 directions)</td></tr>
<tr><td>Noise durability</td><td colspan="5">By noise simulator 1000Vpp noise voltage,
1μs noise width and 25 to 60Hz noise frequency</td></tr>
<tr><td>Dielectric withstand voltage</td><td colspan="5">1500V AC for 1 minute acorss AC external terminals and ground</td></tr>
<tr><td>Insulation resistance</td><td colspan="5">5MΩ or larger by 500V DC insulation resistance tester across batch of AC external terminals and ground</td></tr>
<tr><td>Operating ambience</td><td colspan="5">Free of corrosive gases. Dust should be minimal.</td></tr>
<tr><td>Cooling method</td><td colspan="5">Self-cooling</td></tr>
</table>

Table 3.1 General Specifications

REMARKS

One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10Hz to 20Hz, from 20Hz to 40Hz, from 40Hz to 20Hz, and 20Hz to 10Hz are referred to as one octave.

3. SPECIFICATIONS

3.2 Performance Specifications

The AD61 is used to count pulses which are occuring at a frequency too high for the CPU counters to use. The AD61 counts independently of the CPU.

3.2.1 Performance list

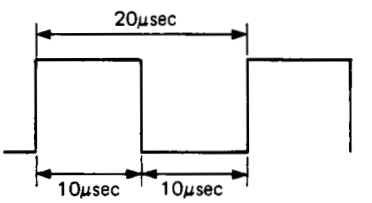
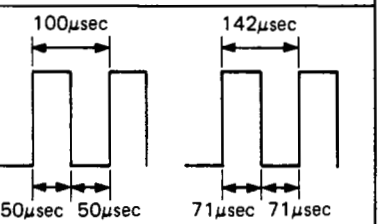
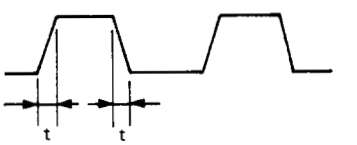
Item			Specifications	
			AD61	AD61S1
I/O points			32 points	
Number of channels			2 channels	
Performance specifications of 1 channel	Count input signal	Phase	1 phase input, 2 phase input	
		Signal level (Phase A, Phase B)	5V DC 12V DC 24V DC } 2 to 5mA	
	Counter	Counting speed *(Maximum)	1 phase input: 50KPPS 2 phase input: 50KPPS	1 phase input: 10KPPS 2 phase input: 7KPPS
		Counting range	24 bits binary 0 to 16,777,215 (decimal)	
		Form	Up/down preset counter plus ring counter function	
		Minimum count pulse width Set input rise and fall times to 5μsec. or less. Duty ratio: 50%	 (1, 2 phase inputs)	 (1 phase input) (2 phase input)
	Magnitude comparison between CPU and AD61	Comparison range	24 bits, binary	
		Comparison result	Set value < count value Set value = count value Set value > count value	
	External input	Preset	12/24V DC, 3/6mA 5V DC, 5mA	
		Count disable	12/24V DC, 3/6mA 5V DC, 5mA	
	External output	Coincidence output	Transistor (open collector) output 12/24V DC, 0.5A	
Current consumption			5V DC, 0.3A	
Weight			0.5kg	

Table 3.2 Performance List

*: Counting speed is influenced by pulse rise time and fall time. Countable speeds are as follows. (If a pulse greater than 50μsec. is counted by the AD61, miscounting may occur. In this case, use the AD61S1.)

(1) AD61 (for both 1 and 2 phase inputs)
t = 5μs. 50KPPS
t = 50μs. . . .5KPPS



(2) AD61S1

Rise/Fall Time	1 Phase Input	2 Phase Input
t = 5μs	10KPPS	7KPPS
t = 500μs	500PPS	250PPS

3.2.2 Functions

(1) General description

The AD61 unit counts high-speed pulse input which cannot be used directly of programmable controller CPU. Its size is the same as that of programmable controller I/O unit.
AD61 incorporates a BIN (binary) 24-bit preset counter function which is capable of up/down count, a ring counter function, an internal preset function, an external disable function, a comparison function with BIN 24-bit set value, and a coincidence signal external output function, applicable to two channels.

(2) Block diagram

General operation

CH1 counter counts the pulse train entering its phase A input up or down as appropriate. In order to read a count value from the CPU unit, it is necessary to read the value via the buffer memory. I/O signals to and from the programmable controller CPU are used to control the operation of the counter. The buffer memory is used to store set data, etc. which controls the counter.

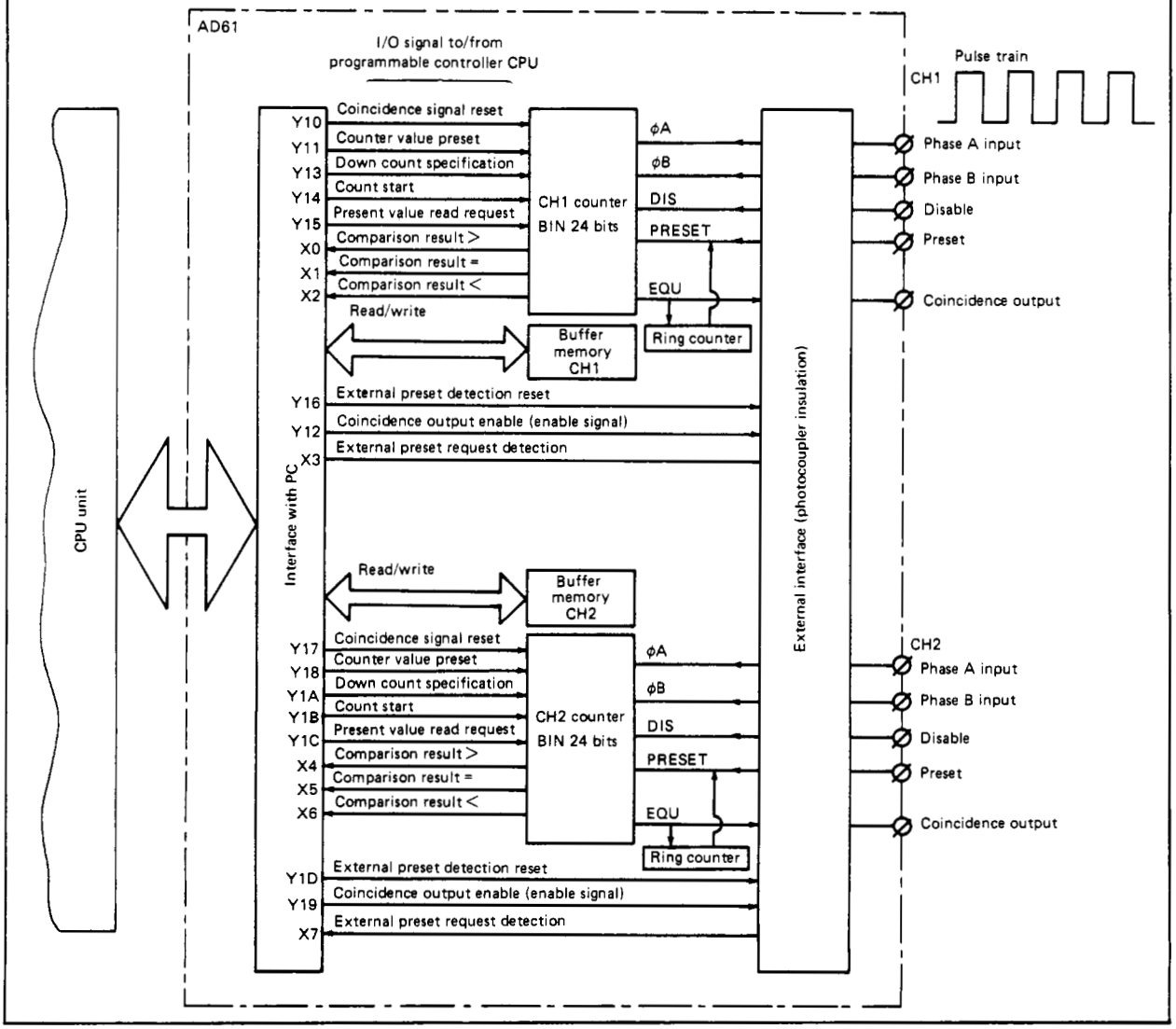
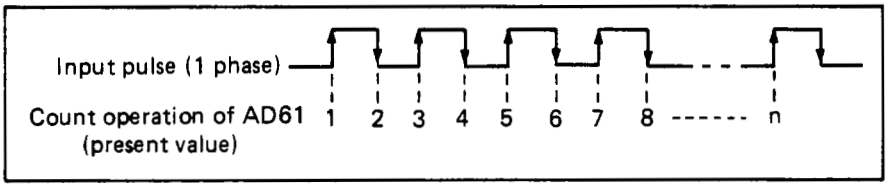


Fig. 3.1 Block Deagram

(3) General description

The AD61 counts the number of input pulses. In the following figure, for example, each time a pulse is input, the AD61 counts pulses in order of 1 to 2 to 3 to 4 to n. The allowable counting range is 0 to 16,777,215. The AD61 unit always executes the comparison function (>, = <) with a set value (a target value optionally set by user).



(4) Pulse input

Pulse inputs may be 1-phase or 2-phase. For 1-phase pulse input, up count (down count specification is also possible from the main program) is made each time a pulse is input. For 2-phase pulse input, the up/down direction of the counter is automatically judged depending on the relation between phase A and phase B. In the following figure, the voltages at the AD61 count input terminal are shown for 1-phase and 2-phase inputs. In this manual, explanation will be given in reference to source load.

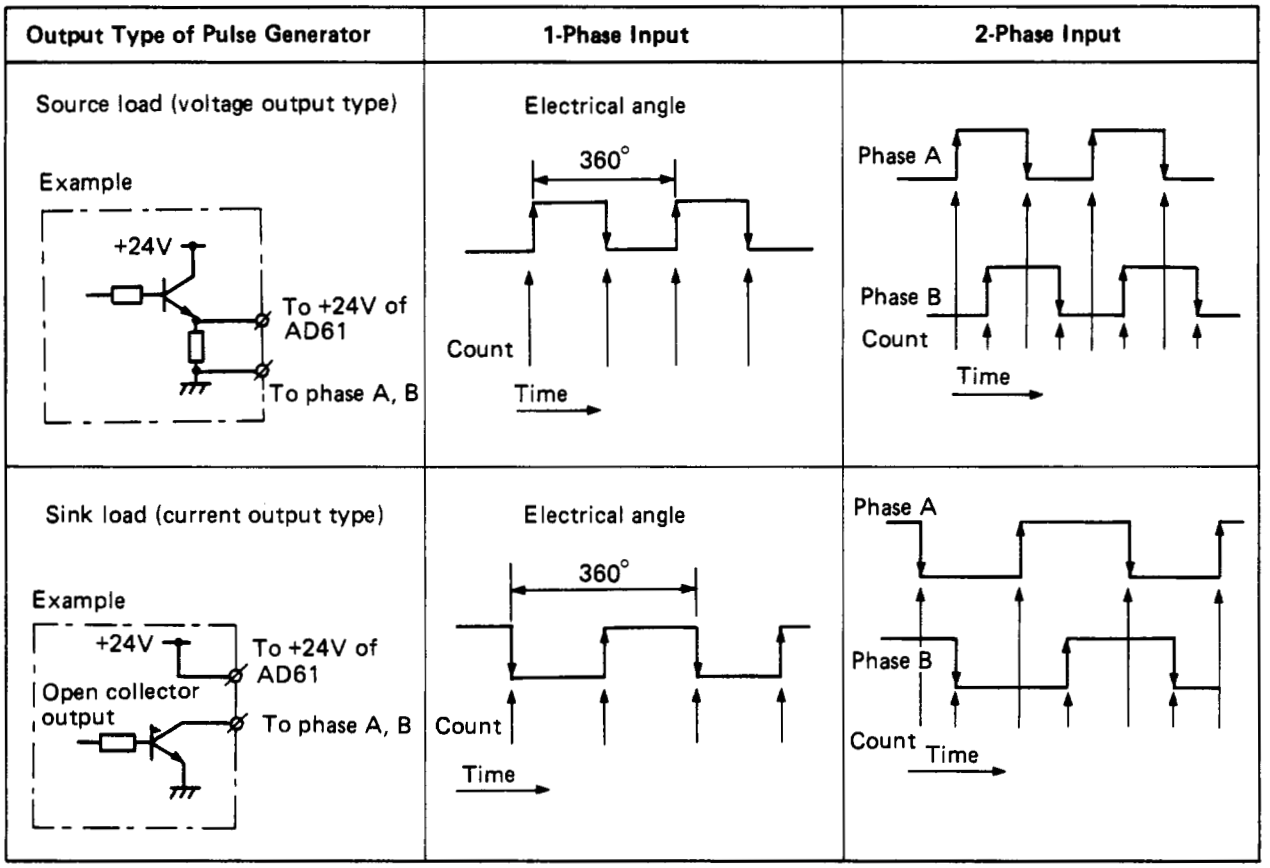


Fig. 3.2 1-Phase and 2-Phase Inputs

(5) Count timing

The timing (for 1 phase input) of the comparison result between a present value and a set value is as indicated below. (Indicated by the assignment numbers of CH1 and 2.)

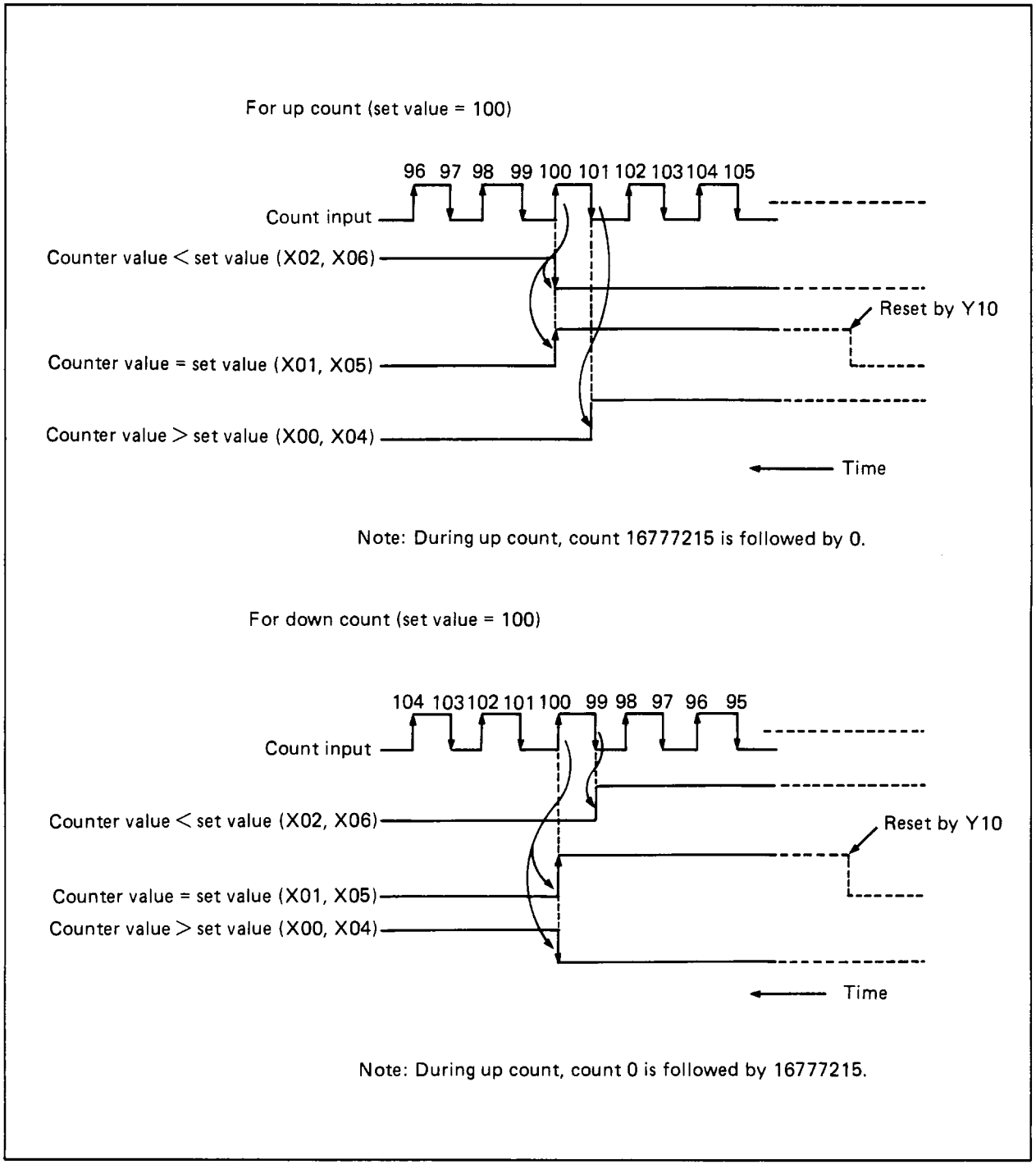


Fig. 3.3 Count Timing

(6) Count mode

On AD61, the count ratios of input pulses are as described below:

1) Twice for 1-phase input (2 counts are made for 1 pulse input).
2) Four times for 2-phase input (4 counts are made for 1 pulse input).

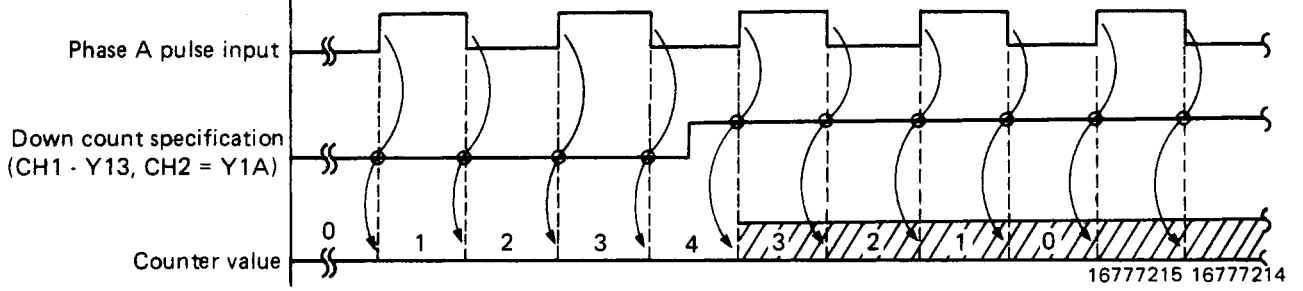
POINT

1. **Each input pulse registers two counts for 1-phase input and four counts for 2-phase input. If the counting range is large, select the pulse generator so that a value twice (for 1 phase) or four times (for 2 phases) greater than the number of generated pulses is within the counting range (0 to 16,777,215).**

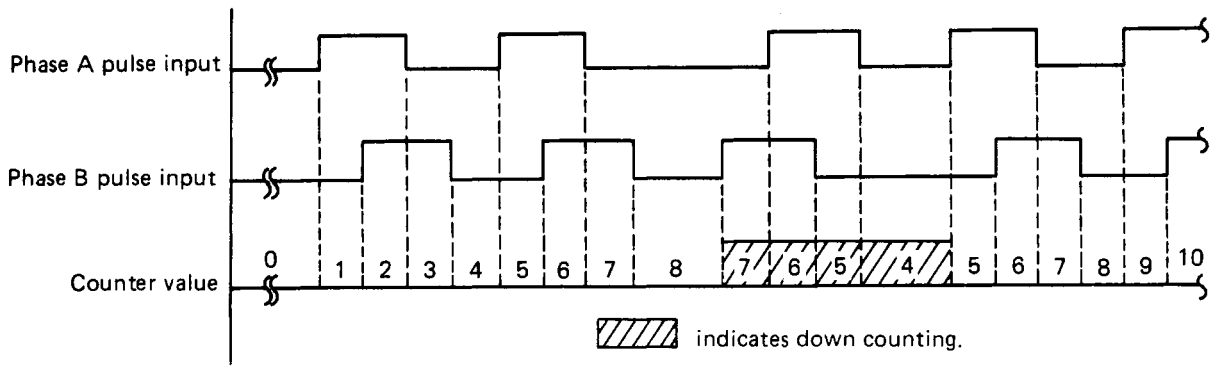
2. **For 1-phase input, specify any set value as twice the actual number of input pulses or halve the present value (by using D/instruction). For 2-phase input, specify any set value as four times the actual number of input pulses or divide the present value by four (by using D/instruction).**

Counting methods for 1-phase input and 2-phase input are shown below. When 1 phase is used, down counting is made if down count specification is on. When 2 phases are used, down count is made if phase B input pulse leads phase A input pulse.

Count timing when 1 phase is used



Count timing when 2 phases are used



(7) Preset function

When the power to the AD61 is turned off, or the CPU reset, the AD61 memory contents are lost (i.e. present values, set values etc.). If these values need to be retained for subsequent use, they must be stored in a suitable data register in the Programmable controller CPU.

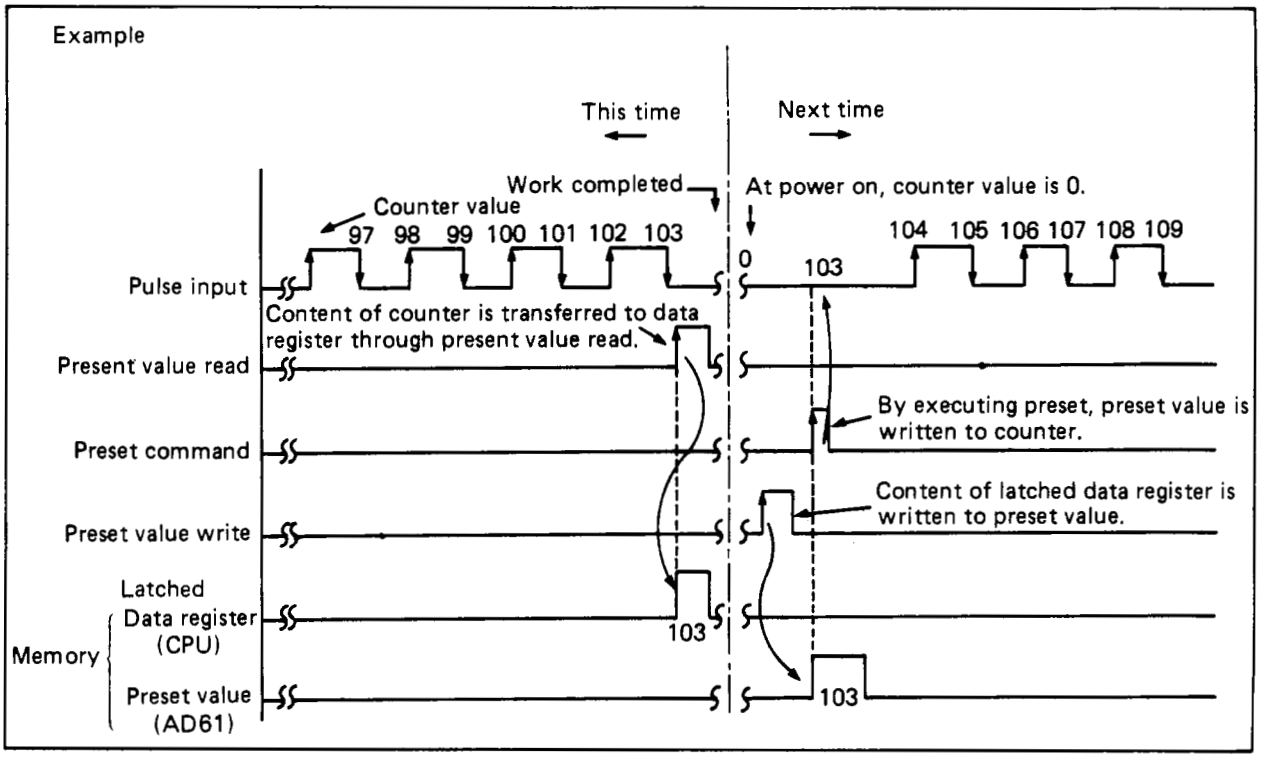


Fig. 3.4 Preset Operation

- The preset value is written to the appropriate buffer memory address (address 1 for CH1, address 33 for CH2) as a 24 bit binary number.
  To load the preset value into the counter current value turn on the preset command (Y 11 for CH1, Y18 for CH2) from the programmable controller CPU.

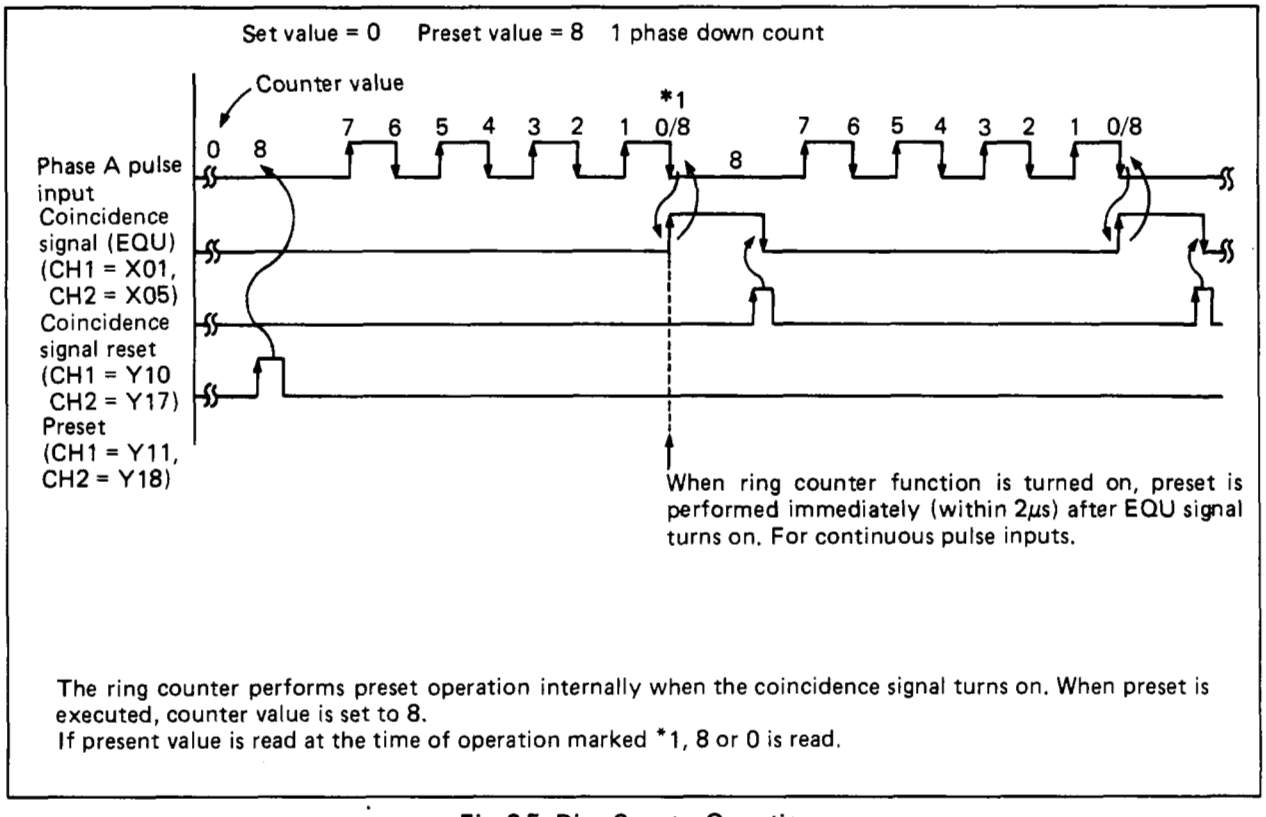
- The preset command may either be loaded from the program or input by applying a voltage to the PRST terminal on the external terminal block (external preset).
  When the external preset signal is given, a flip flop (F/F) is set. If the external preset input turns on again while the F/F is set, the presetting function is stopped. Reset the F/F from the program. (Y16 for CH1, Y1D for CH2) Even if the external preset input remains on, the F/F can be reset. (The F/F is set on the leading edge of the external preset pulse.)

(8) Disable function

By turning on the count enable signal (i.e. a programmable controller I/O signal), AD61 starts counting. (Y14 for CH1, Y1B for CH2)
When a voltage is applied to the DIS (disable) terminal on the external input terminal block, the AD61 stops counting. By utilizing this, counting may be started and stopped by the external input, irrespective of scan time.

(9) Ring counter function

By moving the ring counter setting pin on the AD61 circuit board to the ON position, automatic preset is performed if the counter value becomes equal to the set value. Use this function for cyclic control such as sizing feed. The timing for the ring counter is shown below.



The ring counter performs preset operation internally when the coincidence signal turns on. When preset is executed, counter value is set to 8.
If present value is read at the time of operation marked *1, 8 or 0 is read.

Fig. 3.5 Ring Counter Operation

(10) External output

AD61 is capable of giving a counter value coincidence signal (open collector output) (which turns on if the counter value is equal to the set value). In order to use the counter coincidence signal, it is necessary to turn on the coincidence signal output enable (Y12 for CH1, Y19 for CH2) which is assigned to the programmable controller I/O.

3.3 I/O Signals To and From Programmable Controller CPU

This section describes I/O signals to and from programmable controller CPU when AD61 has been assigned to slot 0.

	CH1	CH2	Signal	Description
Input signal	X00	X04	Counter value greater	Turned on if counter value is greater than set value.
	X01	X05	Counter value coincidence	Latched on if counter value is equal to set value. Turned off by coincidence signal reset command.
	X02	X06	Counter value less	Turned on if counter value is less than set value.
	X03	X07	External preset request detection	Latched on when preset request is given from external input. Turned off when external preset detection signal is reset.

Table 3.3 Input Signals

- Do not use X08 to X0F signals.
- Counter value coincidence signal is turned on when the power is turned on or reset is executed because both the counter value and set value are 0. Therefore, always reset the counter coincidence signal first by turning the coincidence signal reset command on and then off. (If both the counter and set values are 0 after executing the coincidence signal reset command, the counter value coincidence signal is enabled again.)

	Channel		Signal	Operation Timing	Description
	CH1	CH2			
Output signal	Y10	Y17	Coincidence signal reset command		Reset signal for counter value coincidence signal (latch) and coincidence output (EQU) signal
	Y11	Y18	Preset command		Preset value write execution signal
	Y12	Y19	Coincidence signal output enable		By turning on this signal, counter value coincidence signal is output to outside.
	Y13	Y1A	Down count command		If this signal is on in 1 phase mode, down count is performed.
	Y14	Y1B	Count enable		By turning on this signal, count operation is enabled.
	Y15	Y1C	Present value read request		At the rise of this signal, count value is read as present value.
	Y16	Y1D	External preset detection reset command		Reset signal of external preset request detection signal (latch)

Table 3.4 Output Signals

IMPORTANT

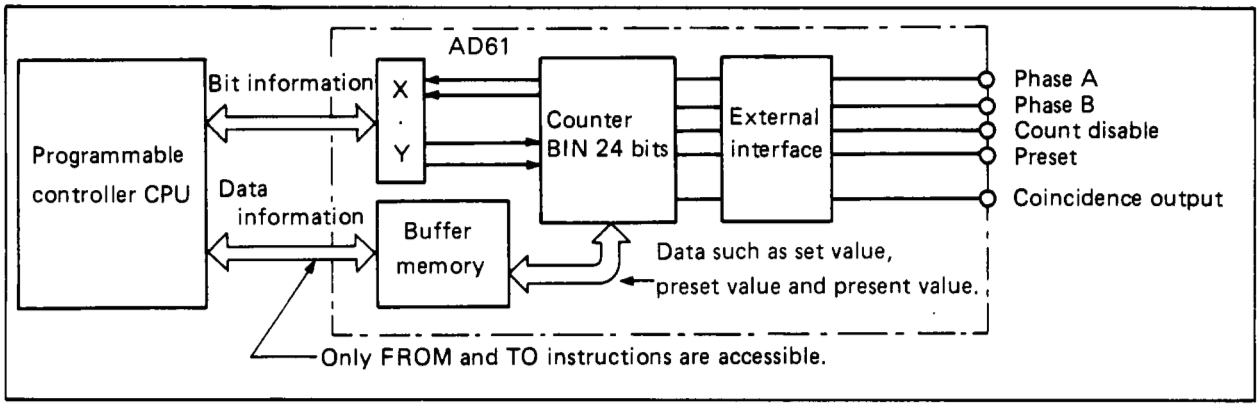
Y00 to 0F and Y1E to 1F may not be used as they are reserved. If one of the above signals is used (turned on/off) in a sequence program, the functions of the AD61 cannot be guaranteed. However, when the AD61 is used for remote I/O, Y0E and Y0F may be reset from the program. (For details, refer to Section 6.3.)

- In Table 3.4 the symbol ⌐¯¯¯

3.4 Buffer Memory

(1) General description

By using FROM and TO instructions, the AD61 is capable of making data communication with the programmable controller CPU through the buffer memory. (The address consists of 16 bits.)



(2) Memory map

The memory map inside the buffer memory is shown below. When the power is turned on or the CPU is reset, the contents of the buffer memory are initialized to 0. Preset value, present value, and set value and handled as 24 bit binary. (The address is expressed in decimal.)

CH1 address	CH2 address		
1	33	Preset value write (lower and middle)	Write only
(2)	(34)	Preset value write (upper)	
3	35	Mode register	Read/write
4	36	Present value read (lower and middle)	Read only
(5)	(37)	Present value write (upper)	
6	38	Set value read/write (lower and middle)	Read/write
(7)	(39)	Set value read/write (upper)	

Addresses in parentheses in the above table indicate those of the upper 8 bits of 24-bit data.

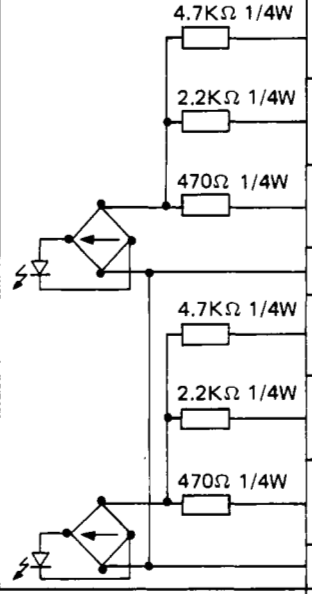
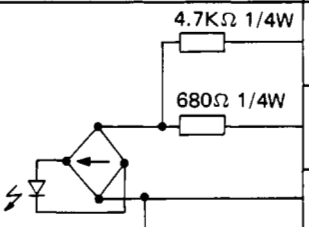
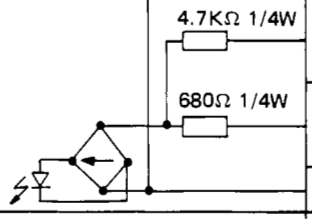
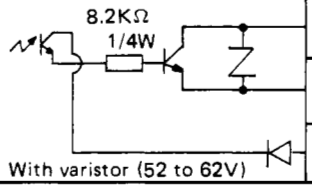
(3) Setting of mode register

Set the value of the mode register as indicated in the following table. The value is indicated in decimal.
When the power is turned on, the value is 0.

Division of Phase	Data to Be Written
1 phase	8
2 phases	18

3.5 Interface with External Equipment

The external equipment interface list of AD61 is indicated below.

I/O Division	Internal Circuit	Terminal Number CH1	Terminal Number CH2	Signal	Operation	Input Voltage (Guaranteed value)	Operation Current (Guaranteed value)
*Input		1	19	Phase A pulse input 24V	At ON	21.6 to 26.4V	2 to 5mA
					At OFF	5V or less	0.1mA or less
		2	20	Phase A pulse input 12V	At ON	10.8 to 13.2V	2 to 5mA
					At OFF	4V or less	0.1mA or less
		3	21	Phase A pulse input 5V	At ON	4.5 to 5.5V	2 to 5mA
					At OFF	2V or less	0.1mA or less
		4	22	COM			
		5	23	Phase B pulse input 24V	At ON	21.6 to 26.4V	2 to 5mA
					At OFF	5V or less	0.1mA
		6	24	Phase B pulse input 12V	At ON	10.8 to 13.2V	2 to 5mA
					At OFF	4V or less	0.1mA or less
		7	25	Phase B pulse input 5V	At ON	4.5 to 5.5V	2 to 5mA
					At OFF	2V or less	0.1mA or less
		8	26	COM			
Input		9	27	Disable input 12/24V	At ON	10.2 to 26.4V	2 to 6mA
					At OFF	2V or less	0.1mA or less
		10	28	Disable input 5V	At ON	4.5 to 5.5V	3.5 to 5.5mA
					At OFF	1.5V or less	0.1mA or less
		11	29	COM	Response time	OFF → ON 0.5ms	ON → OFF 3ms or less
Input		12	30	Preset input 12/24V	At ON	10.2 to 26.4V	2 to 6mA
					At OFF	2V or less	0.1mA or less
		13	31	Preset input 5V	At ON	4.5 to 5.5V	3.5 to 5.5mA
					At OFF	1.5V or less	0.1mA or less
		14	32	COM			
Output		15	33	EQU Open collector	Operating voltage: 10.2 to 30V Rated voltage: 0.5A Maximum rush current: 4A, 10msec Maximum voltage drop at ON: 1.5V at 0.5A Response time: OFF → ON 0.1msec or less (Resistor load) ON → OFF 0.1msec or less		
		16	34	COM			
		17	35	12/24V external power input	Input voltage: 10.2 to 30V Current consumption: 2 to 5mA		

4. HANDLING

This chapter describes the handling instructions, nomenclature, maintenance, and inspection of the AD61.

4.1 Handling Instructions

(1) Protect the AD61 and its terminal block from impact.

(2) Do not touch or remove the printed circuit board from the case.

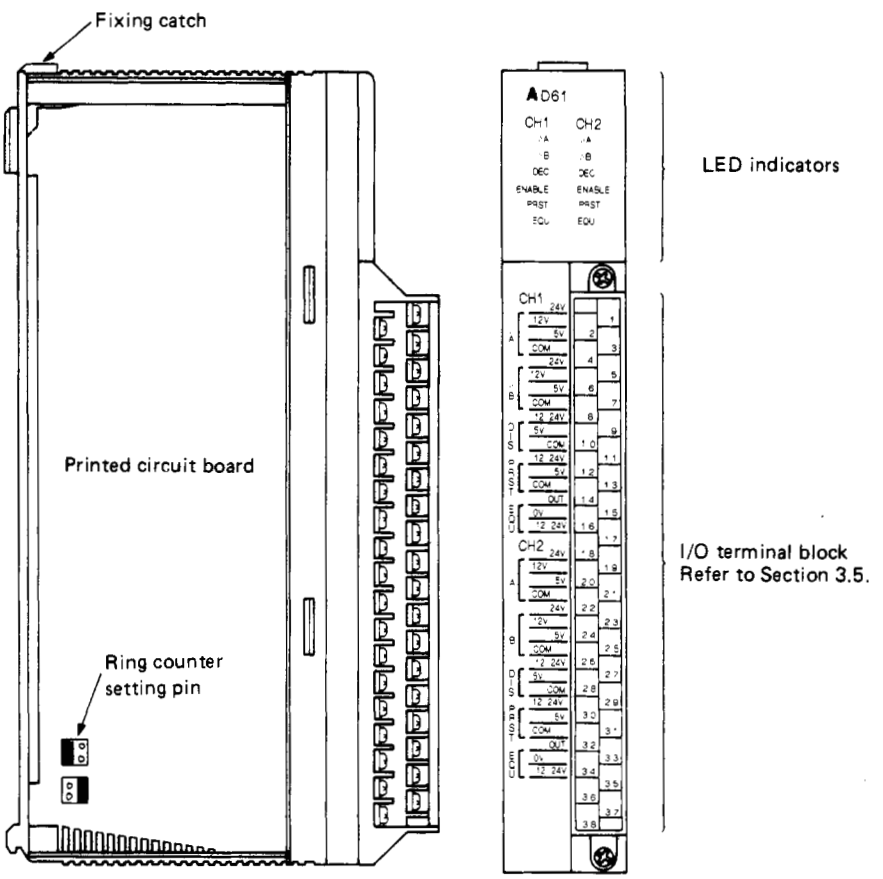
(3) When wiring, ensure that no wire offcuts enter the unit and remove any that do enter.

(4) Tighten terminal screws as specified below.

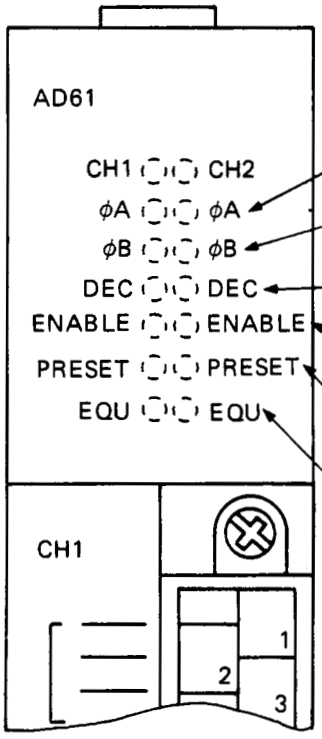
Screw	Tightening Torque Range (kg·cm)
I/O terminal block terminal screw (M3 screw)	5 to 8
I/O terminal block mounting screw (M4 screw)	8 to 14

(5) To load the unit onto the base, press the unit against the base so that the hook is securely locked. To unload the unit, push the catch on the top of the unit, and after the hook is disengaged from the base, pull the unit toward you.

4.2 Nomenclature and Explanation



(1) LED indicators: LED "on" conditions are explained below. LED operations of CH1 are the same as those of CH2.



Phase A pulse input indicator
(Lit when voltage is applied to phase A pulse input terminal)

Phase B pulse input indicator
(Lit when voltage is applied to phase B pulse input terminal)

Down count indicator

Count input acceptable
(Lit when disable input is off and internal output count enable is on)

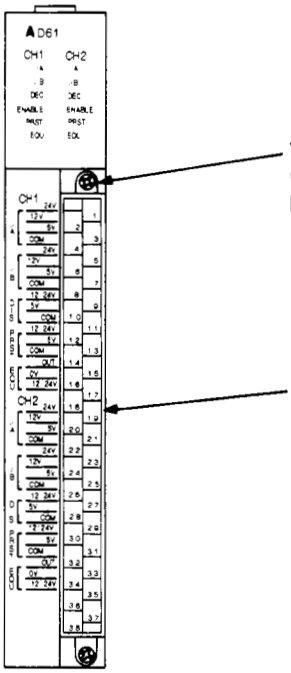
* External preset input detection
(Lit and latched when voltage is applied to preset input terminal)

External coincidence output operation
(Lit when counter value coincidence signal is on and external output enable is on)

REMARKS

*If external preset detection reset signal (Y16 for CH1, Y1D for CH2) is turned on when this LED is on, it will turn off.

(2) I/O terminal block: I/O terminal block is explained below. For the arrangement of terminal block, refer to Section 3.5.



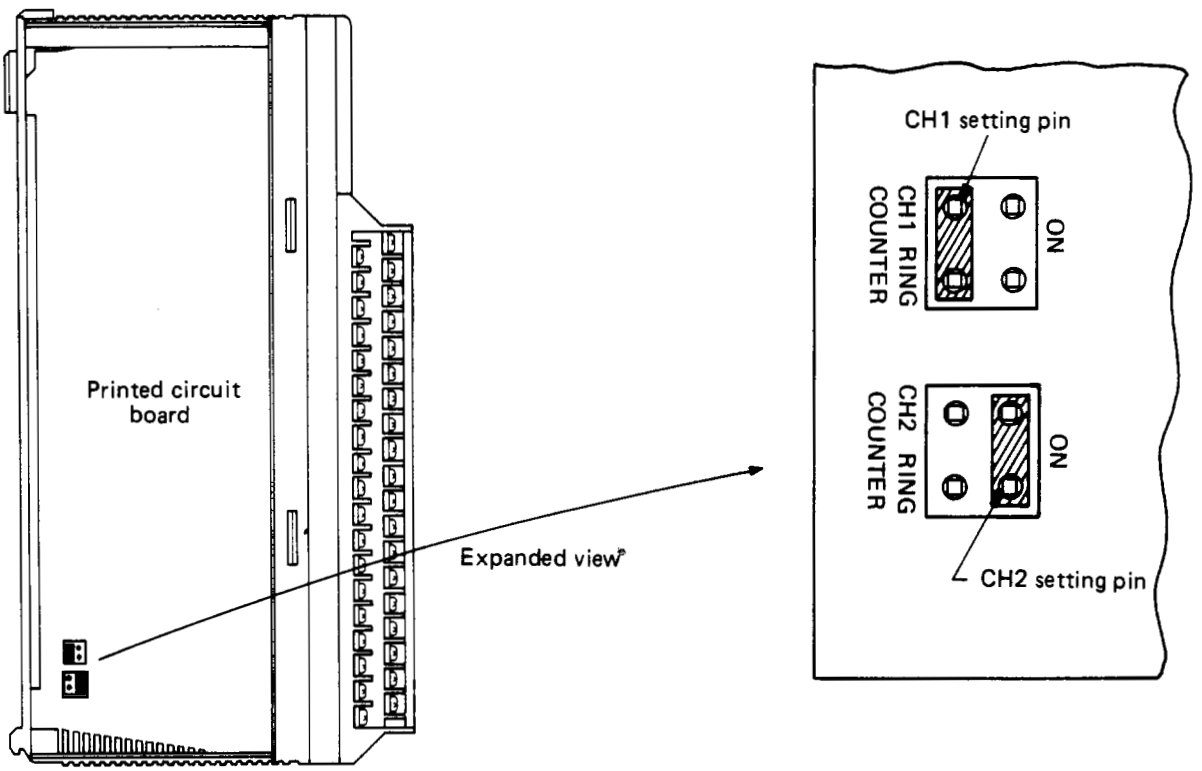
Terminal block mounting screw
By loosing this screw, the terminal block can be removed from unit.

Terminal block cover

4.3 Setting of Ring Counters

To select the ring counter function, change the setting of the pin on the circuit board. As shown below, ring counter setting pins are located AD61 at the bottom left of the circuit board.

Set the ring counters individually for CH1 and CH2. The pins are factory-set at the OFF position. (If the pin is removed, setting is placed into OFF state.) The figure shows CH1 ring counter OFF and CH2 ring counter ON.



4.4 Maintenance

For general maintenance and inspection items, to the A CPU User's Manual.
Since the AD61 uses an external power supply, check that the external power voltage is within ±10% of the rated voltage every three to six months.

5. WIRING AND INSTALLATION

5.1 Unit Arrangement Precautions

Only use the AD61 on an extension base which has a power supply unit installed. Do not use the AD61 on an extension base which does not have a power supply unit because power capacity may become insufficient.

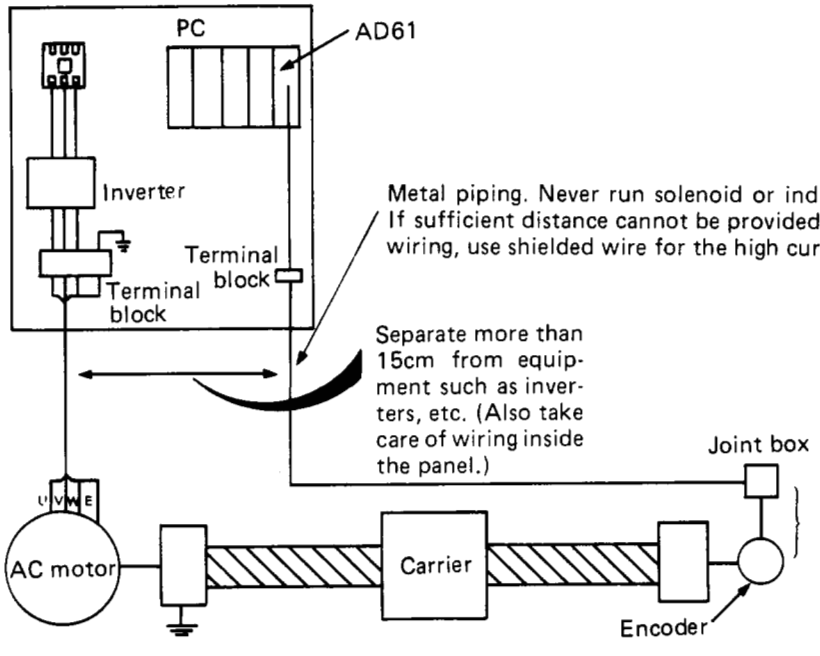
5.2 Wiring

5.2.1 Wiring instructions

When using high speed pulse inputs take precautions against noise in all wiring.

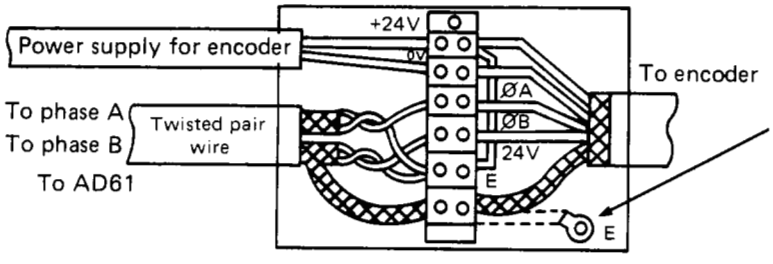
1) Be sure to use shielded twisted pair wires. Also provide Class 3 grounding.
2) Do not run a twisted pair wire in parallel with any power line, I/O line, etc. which may generate noise. It is necessary to run the twisted pair wire separately from the above described lines and over the shortest possible distance.
3) A stabilized power supply is necessary for the pulse generated. For 1-phase input, connect count input signal only to phase A. For 2-phase input, connect count input signal to phase A and phase B.

Special care must be taken to prevent the input wiring from picking up noise. The diagram below indicates the type of precautions required.


PC
AD61
Inverter
Terminal block
Terminal block
Metal piping. Never run solenoid or inductive wiring through the same conduit. If sufficient distance cannot be provided between the high current line and input wiring, use shielded wire for the high current line.
Separate more than 15cm from equipment such as inverters, etc. (Also take care of wiring inside the panel.)
Joint box
U V W E
AC motor
Carrier
Encoder

Distance between encoder and joint box should be as short as possible. If the distance from the AD61 to the encoder is too long an excessive voltage drop occurs. Therefore, measure the voltage during operation and check that the voltages are within the rated voltage of the encoder. If the voltage drop is large, increase the size of wiring or use an encoder of 24V DC with less current consumption.

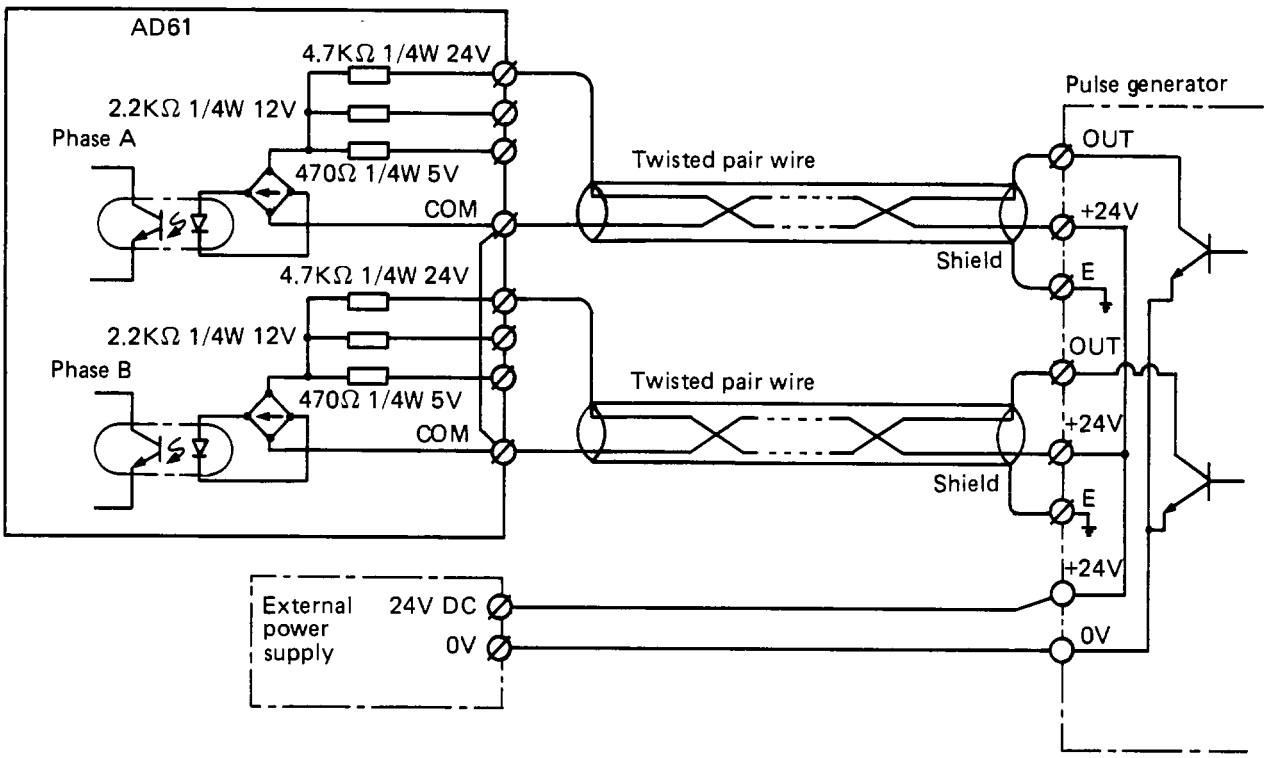
●Ground twisted shield wire on the encoder side (joint box). (This is a connection example for 24V sink load.)



Connect the encoder shield wire to the twisted pair shield wire inside the joint box. If the shield wire of the encoder is not grounded in the encoder, ground it inside the joint box as indicated by dotted line.

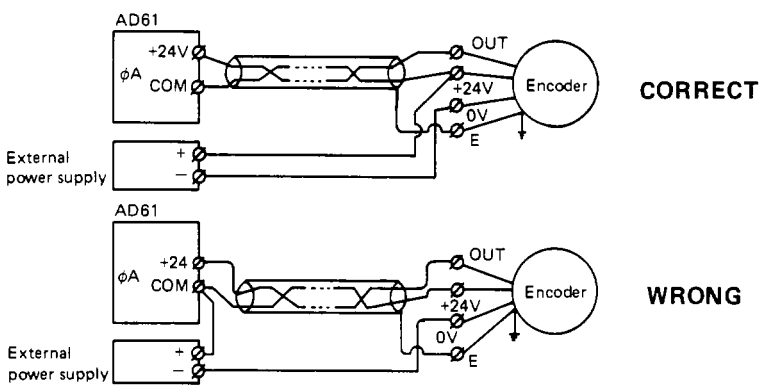
5.2.2 Unit wiring examples

(1) Pulse generator is open collector output (24V DC)

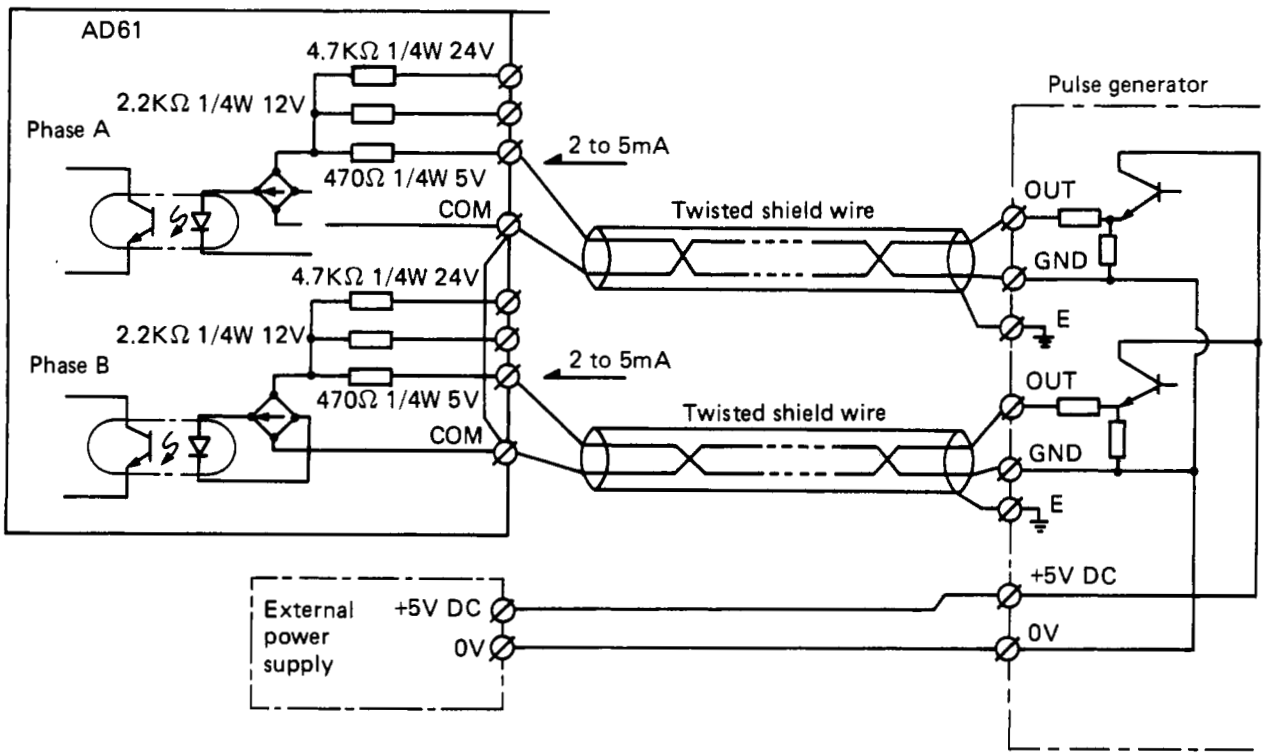


POINT

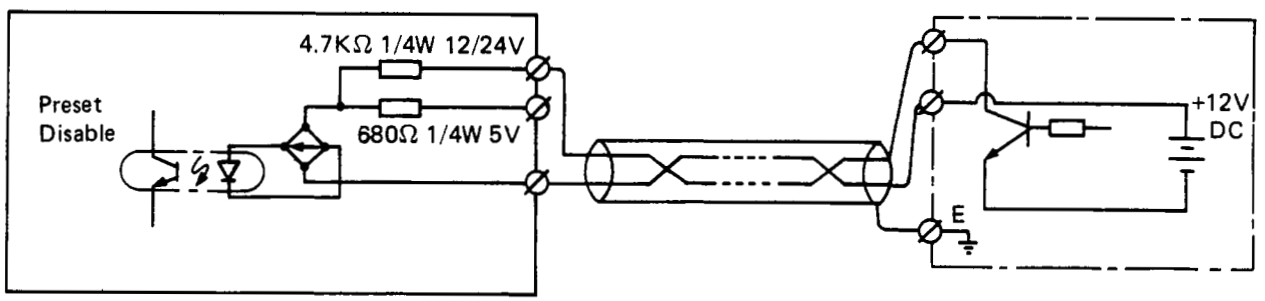
In order to minimize any interference from noise on the encoder power supply, the encoder signal and supply lines should be wired as follows:



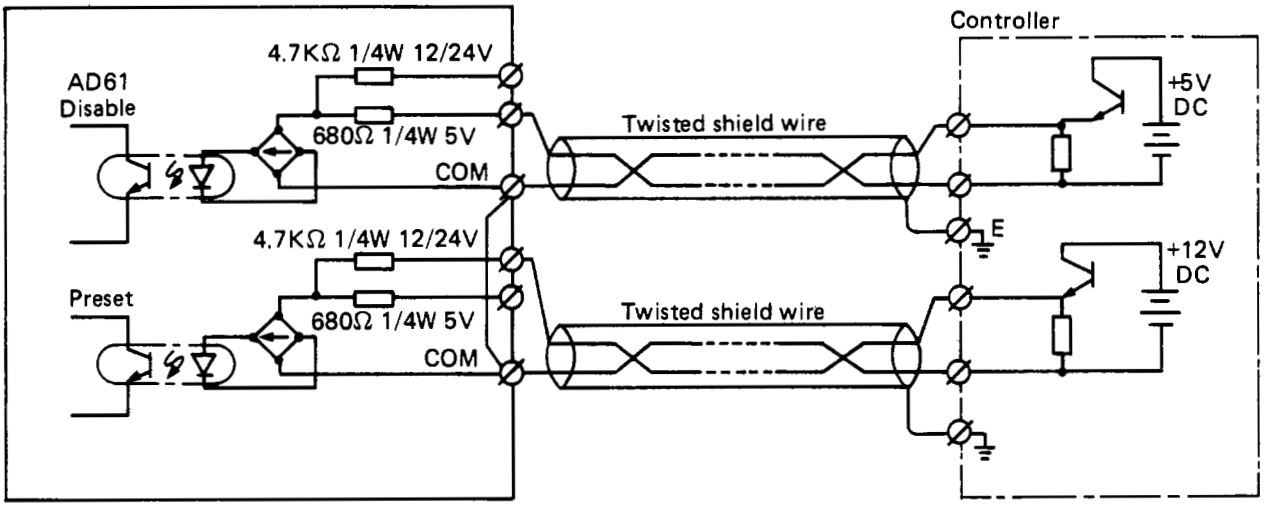
(2) Pulse generator is voltage output type (5V DC)



(3) Connection with input (the same interface for preset and disable)

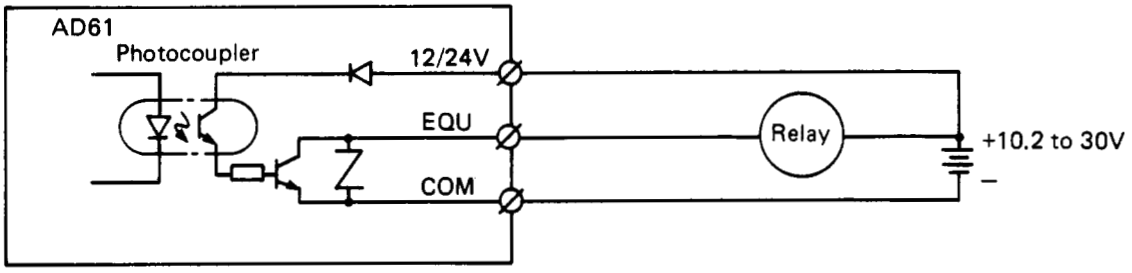


(4) Source load (voltage output type)



(5) Connection with EQU terminal

To use the EQU terminal, the internal photocoupler should be activated. For this purpose, 10.2 to 30V external power is necessary. Connection methods are as follows:



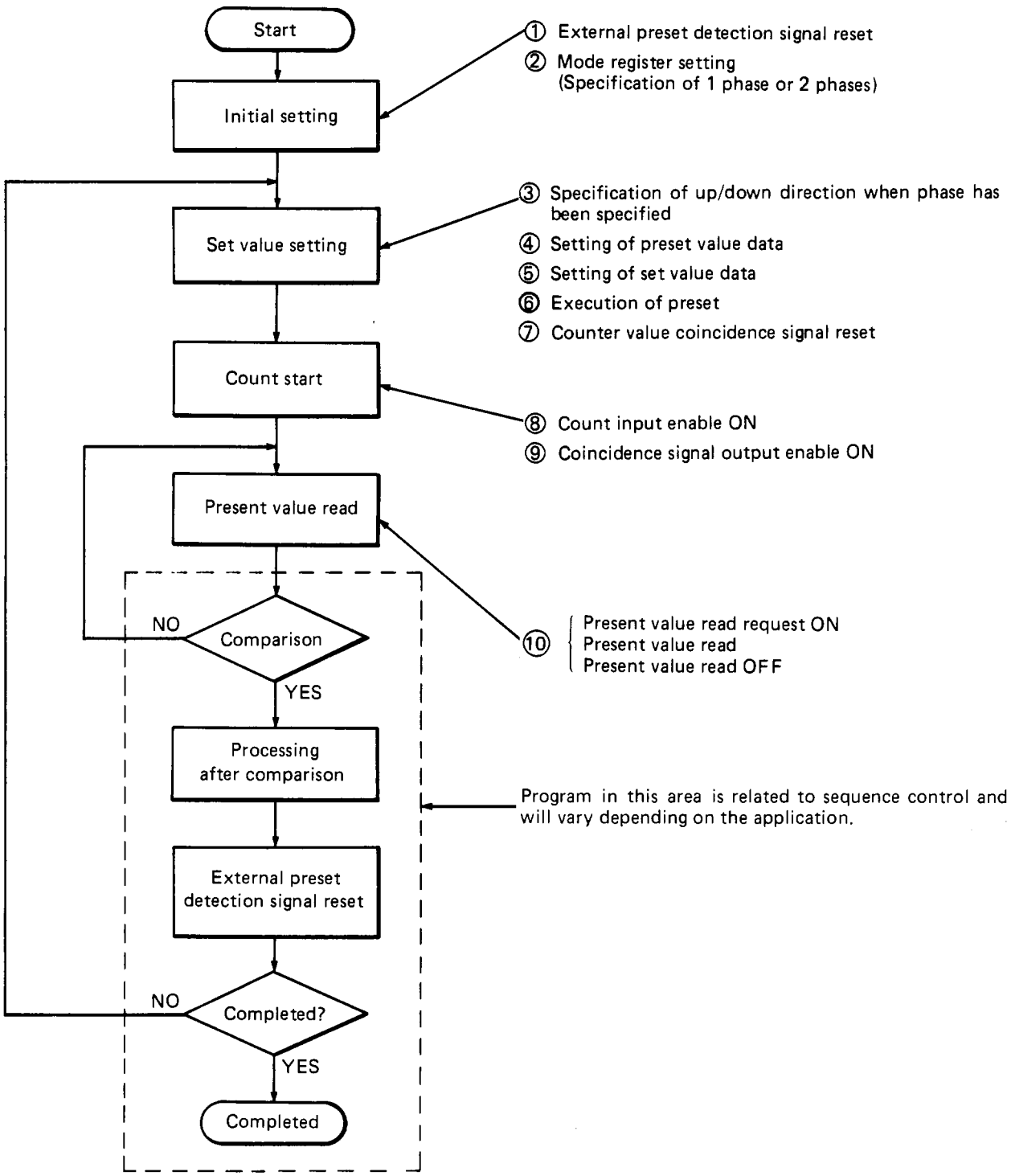
6. PROGRAMMING

6.1 General Description of Programming

Program flow for the control of AD61 is as shown below. (Common to A0J2, A1, A2, A3CPU)

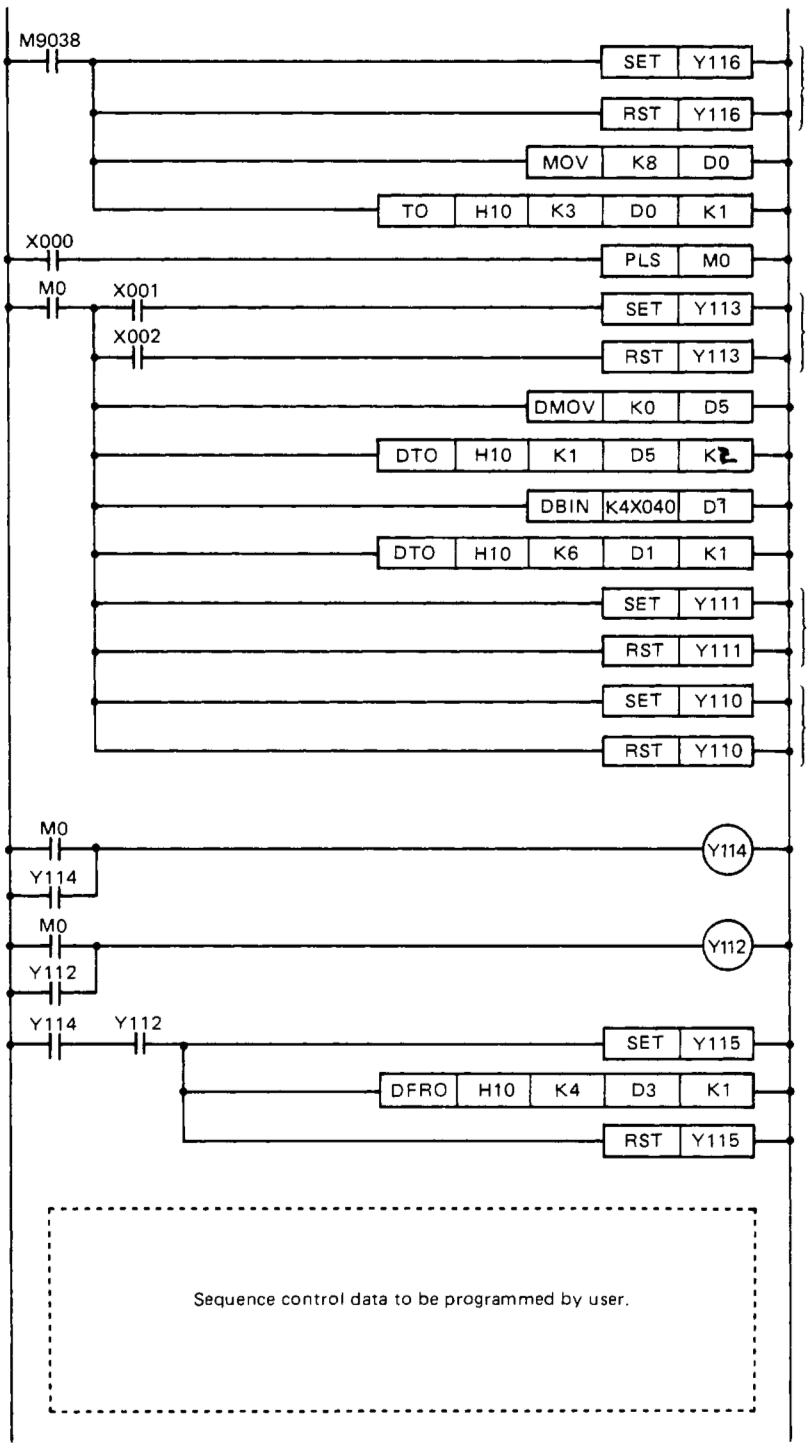
(1) Flow chart and programming procedure when ring counter function is not used

1) Flow chart


Start
Initial setting
Set value setting
Count start
Present value read
NO
Comparison
YES
Processing after comparison
External preset detection signal reset
NO
Completed?
YES
Completed
① External preset detection signal reset
② Mode register setting (Specification of 1 phase or 2 phases)
③ Specification of up/down direction when phase has been specified
④ Setting of preset value data
⑤ Setting of set value data
⑥ Execution of preset
⑦ Counter value coincidence signal reset
⑧ Count input enable ON
⑨ Coincidence signal output enable ON
⑩ Present value read request ON
Present value read
Present value read OFF
Program in this area is related to sequence control and will vary depending on the application.

2) Programming procedure

The following example shows the programming procedure for the A1, A2, and A3CPUs according to the flow chart in 1). The AD61 I/O numbers are assigned to 100 to 11F.



*1
1) External preset detection reset

2) Writes 1 phase constant to data register
Writes mode to buffer memory

*1
3) Up/down count direction setting

4) Writes preset value (0) to data registers (D5, D6)
Writes preset value to buffer memory

5) Reads set value from digital switch to data registers (D1, D2). (The set value should be twice the required pulse input.)
Writes set value to buffer memory

*1
6) Preset command

*1
7) Coincidence signal reset

8) Count enable

9) Coincidence signal output enable (necessary for output to EQU terminal)

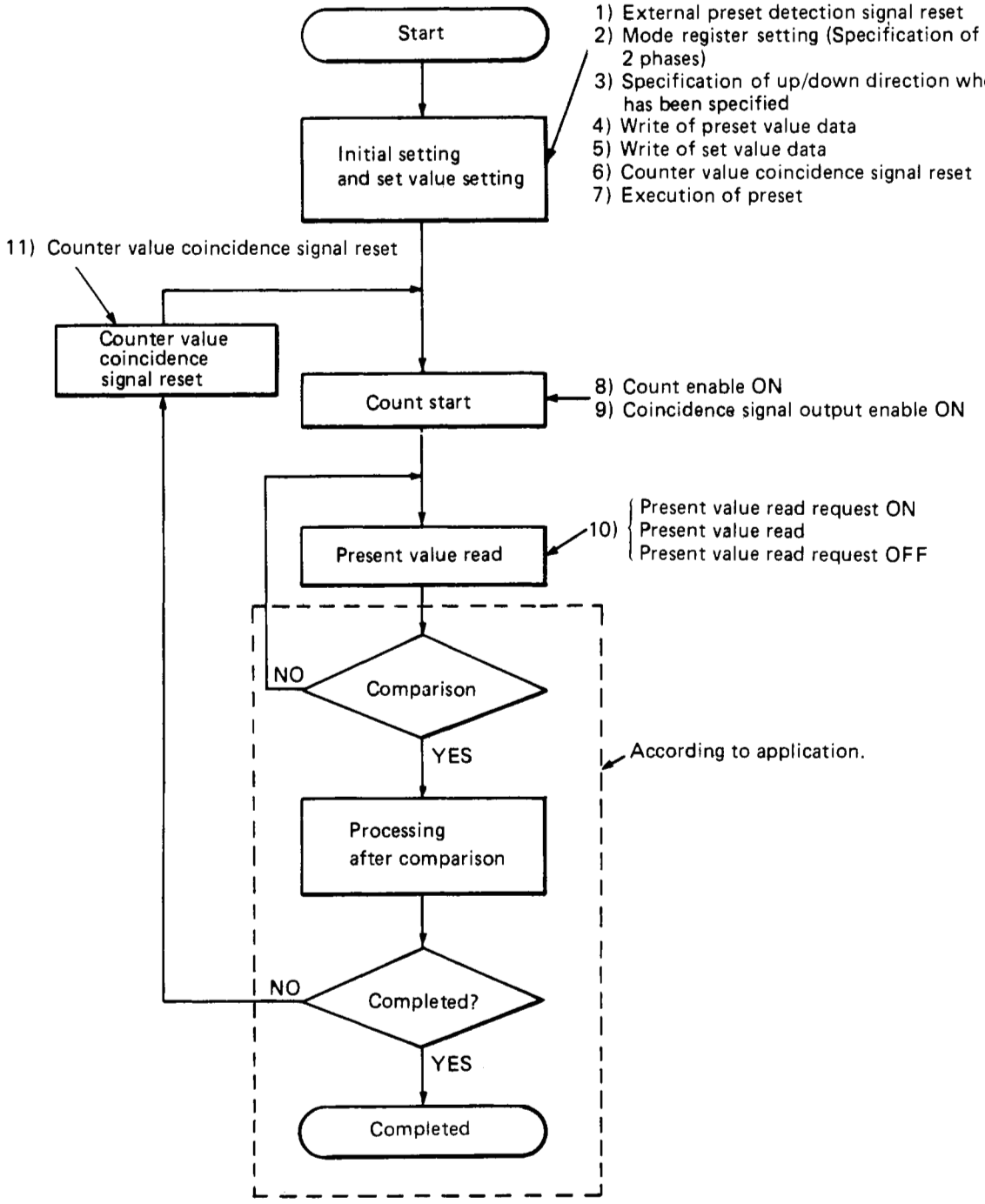
*1
10) Present value read request
Reads present value from buffer memory to data registers (D3, D4)

POINT

***1: When using the A1E, A2E, or A3ECPU, use the partial refresh instructions.**

(2) Flow chart and programming procedure when ring counter function is used

1) Flow chart

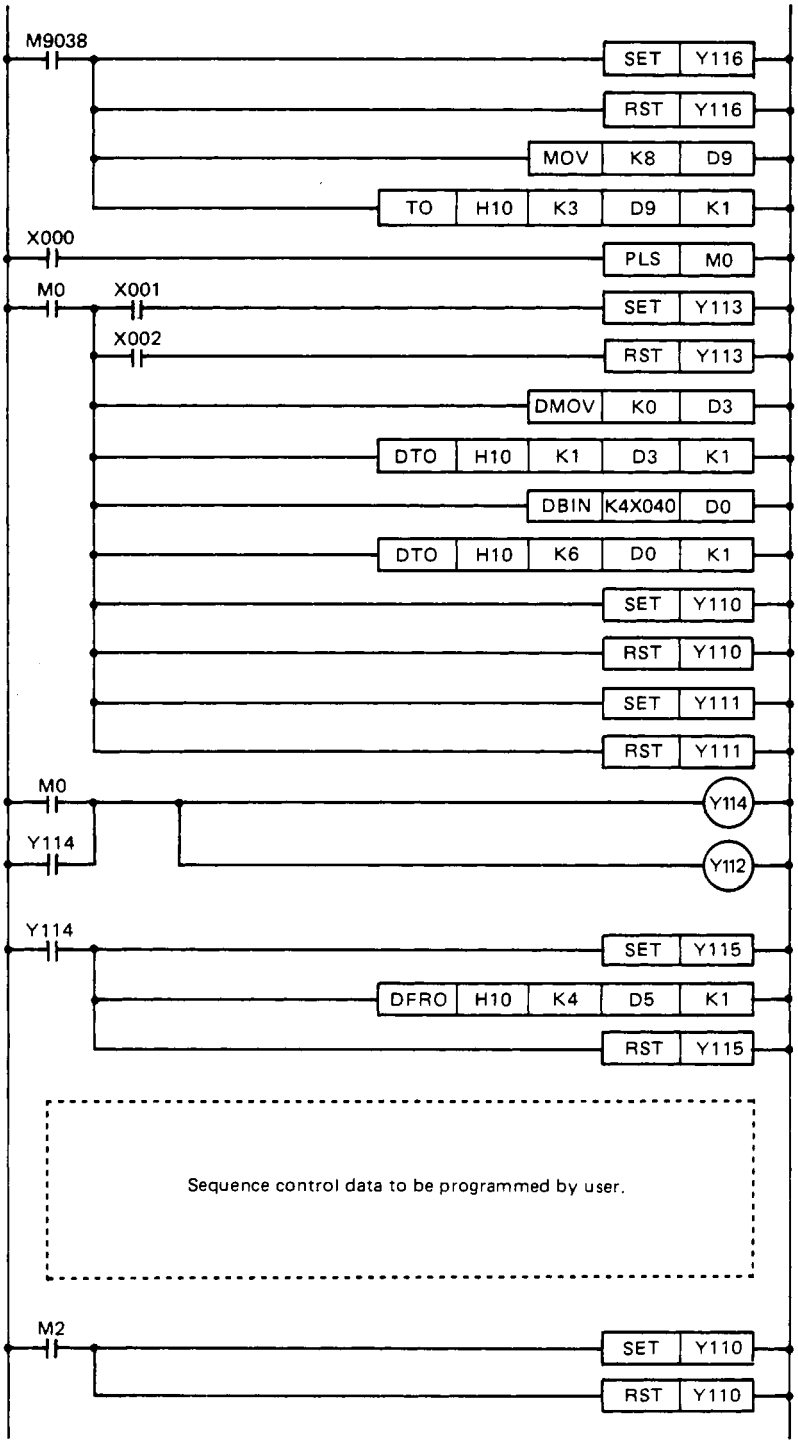

Start
Initial setting and set value setting
1) External preset detection signal reset
2) Mode register setting (Specification of 1 phase or 2 phases)
3) Specification of up/down direction when 1 phase has been specified
4) Write of preset value data
5) Write of set value data
6) Counter value coincidence signal reset
7) Execution of preset
11) Counter value coincidence signal reset
Counter value coincidence signal reset
Count start
8) Count enable ON
9) Coincidence signal output enable ON
Present value read
10) Present value read request ON
Present value read
Present value read request OFF
NO
Comparison
YES
According to application.
Processing after comparison
NO
Completed?
YES
Completed

POINT

When the ring counter function is used, the next preset cannot be performed if the counter coincidence signal (X01 for CH1, X05 for CH2) remains on. Be sure to reset the counter coincidence signal.

2) Programming procedure

The following example shows the programming procedure for the A1, A2, and A3CPUs according to the flow chart in 1). The AD61 I/O numbers are assigned to 100 to 11F.



*1
1) External preset detection reset

2) Writes 1 phase constant to data register
Writes mode to buffer memory

*1
3) Up/down count direction setting

4) Writes preset value (0) to data registers (D3, D4)
Writes preset value to buffer memory

5) Reads set value from digital switch to data registers (D1, D2). (The set value should be twice the required pulse input.)
Writes set value to buffer memory

*1
6) Coincidence signal reset

*1
7) Preset command

8) Count enable

9) Coincidence signal output enable (necessary for output to EQU terminal)

High speed command ON

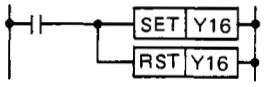
*1
10) Present value read request
Reads present value from buffer memory to data registers (D5, D6)

*1
11) Coincidence signal reset

POINT

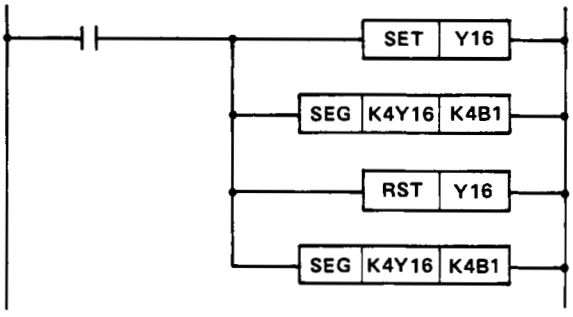
***1: When using the A1E, A2E, or A3ECPU, use the partial refresh instructions.**

(3) Differences of programming depending on system configurations

System Configuration Using AD61	Instruction or Programming Method Necessary for Use of AD61	
	Accessing method to buffer memory	AD61 F/F reset pulse generating method
A CPU data link system. Remote I/O station	RFRP instruction (equivalent to FROM instruction) RTOP instruction (equivalent to TO instruction) Only one instruction may be executed for 1 special unit within 1 scan.	Since Y output to actual remote I/O station is executed after END of sequence program, pulse is not output by the above method. To output pulse to remote I/O station, create the following program; SET Y16 → END (link refresh) → RST Y16 → END (link refresh).
A CPU in dependent system. A CPU data link system. Master station and local station.	FROM and TO instructions are used.	SET and RST are used. Example:  Use of PLS Y16 turns on Y16 for 1 scan. This is undesirable because AD61 may not operate for that period.

POINT

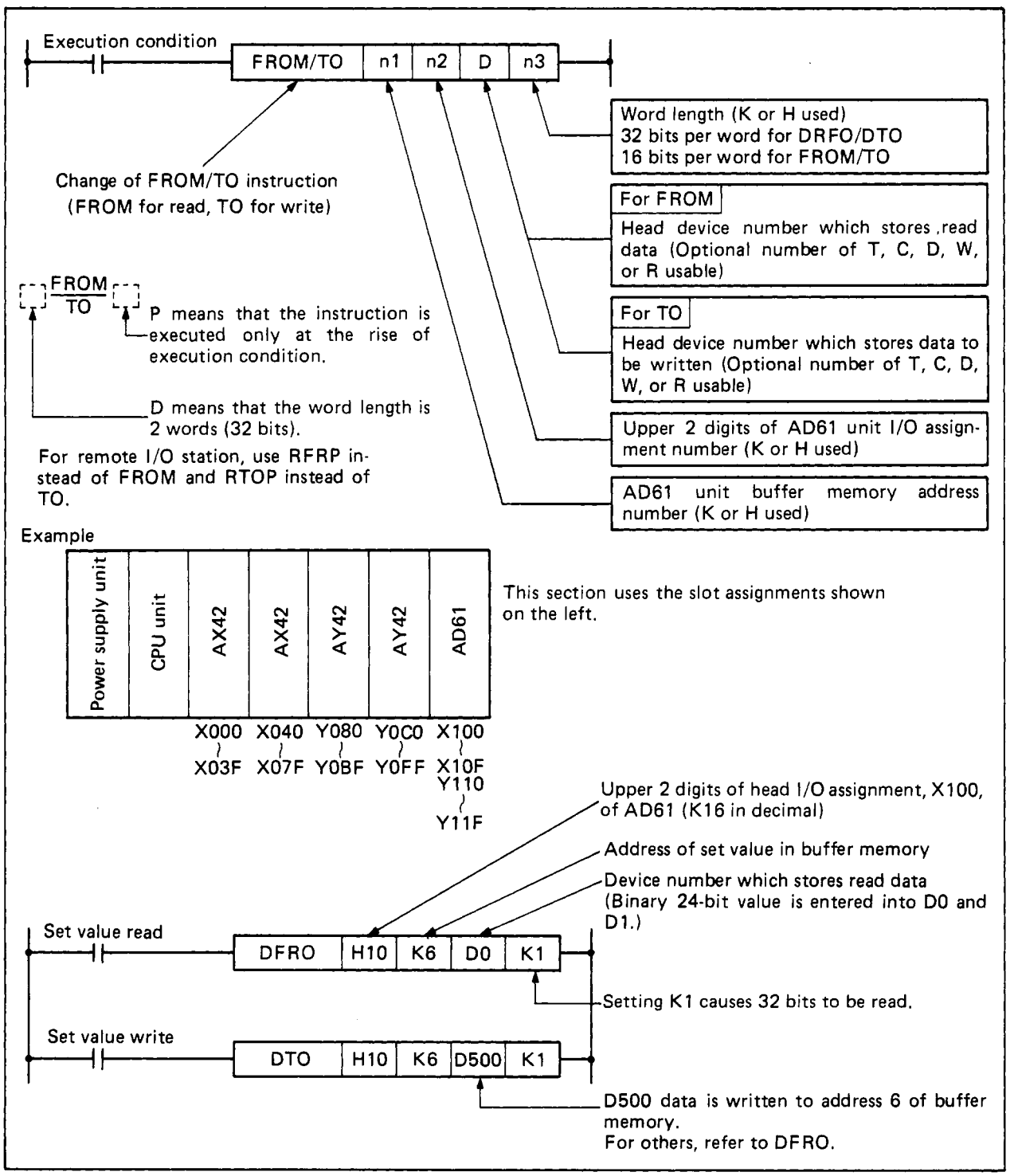
When using the I/O refresh type CPU (A1E, A2E, A3ECPU), always use the partial refresh instructions and convert them into pulses using the SET and RST instructions.



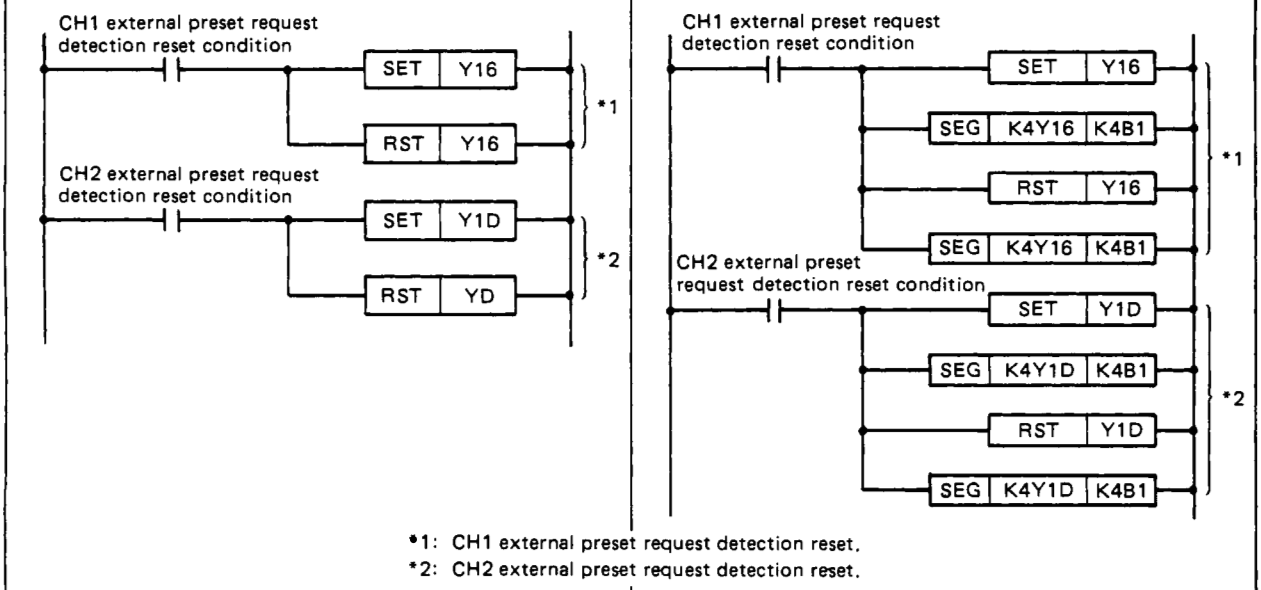
6.2 Programming for A1(E), A2(E) and A3(E)CPU

This section describes the programming procedure for A1(E), A2(E), and A3(E)CPU. Explanation will be given in order of programming flow chart in Section 6.1.

To use any special function unit, utilize FROM and TO instructions. These instructions will be described below. For details, refer to A1, A2, A3 Programming Manual.

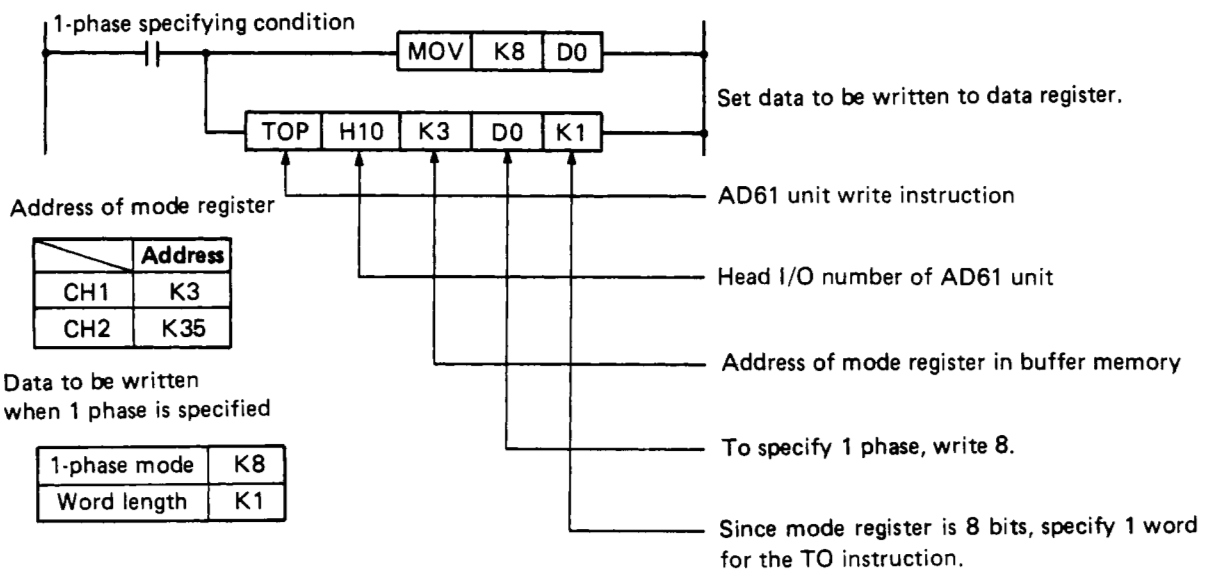

Execution condition
FROM/TO
n1
n2
D
n3
Word length (K or H used)
32 bits per word for DRFO/DTO
16 bits per word for FROM/TO
Change of FROM/TO instruction
(FROM for read, TO for write)
For FROM
Head device number which stores ,read data (Optional number of T, C, D, W, or R usable)
FROM
TO
P means that the instruction is executed only at the rise of execution condition.
For TO
Head device number which stores data to be written (Optional number of T, C, D, W, or R usable)
D means that the word length is 2 words (32 bits).
Upper 2 digits of AD61 unit I/O assignment number (K or H used)
For remote I/O station, use RFRP instead of FROM and RTOP instead of TO.
AD61 unit buffer memory address number (K or H used)
Example
Power supply unit
CPU unit
AX42
AX42
AY42
AY42
AD61
This section uses the slot assignments shown on the left.
X000 X040 Y080 Y0C0 X100
X03F X07F Y0BF Y0FF X10F
Y110
Y11F
Upper 2 digits of head I/O assignment, X100, of AD61 (K16 in decimal)
Address of set value in buffer memory
Device number which stores read data (Binary 24-bit value is entered into D0 and D1.)
Set value read
DFRO
H10
K6
D0
K1
Setting K1 causes 32 bits to be read.
Set value write
DTO
H10
K6
D500
K1
D500 data is written to address 6 of buffer memory.
For others, refer to DFRO.

(1) External preset detection reset



- To perform preset from outside, it is necessary to perform reset of external preset each time.
- Since the preset operation occurs on the pulse leading edge, further, preset by external input or preset by sequence program cannot be performed until the external preset flip flop has been reset.
- The external preset flip flop can be reset while the external preset input is on.
- It is not necessary to execute this signal if the external preset terminal is not used.

(2) Setting of mode register (1-phase specification)


1-phase specifying condition
MOV K8 D0
Set data to be written to data register.
TOP H10 K3 D0 K1
AD61 unit write instruction
Address of mode register
Head I/O number of AD61 unit
Address of mode register in buffer memory
To specify 1 phase, write 8.
Since mode register is 8 bits, specify 1 word for the TO instruction.

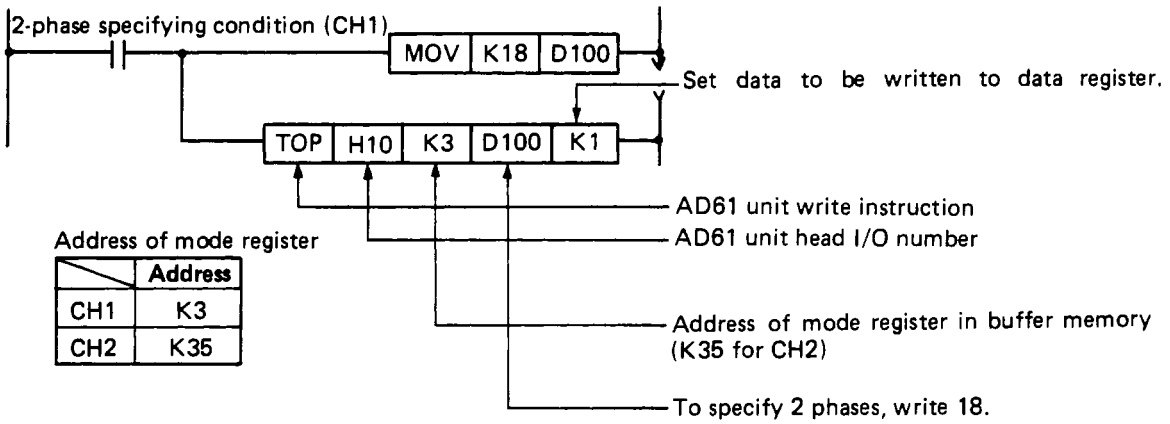
	Address
CH1	K3
CH2	K35

Data to be written when 1 phase is specified

1-phase mode	K8
Word length	K1

- When the power is turned on or the CPU is reset, the value of the mode register is 0.
- For the specification of up or down count, refer to Section (4).

(3) Setting of mode register (2-phase specification)


2-phase specifying condition (CH1)
MOV K18 D100
Set data to be written to data register.
TOP H10 K3 D100 K1
AD61 unit write instruction
AD61 unit head I/O number
Address of mode register in buffer memory (K35 for CH2)
To specify 2 phases, write 18.

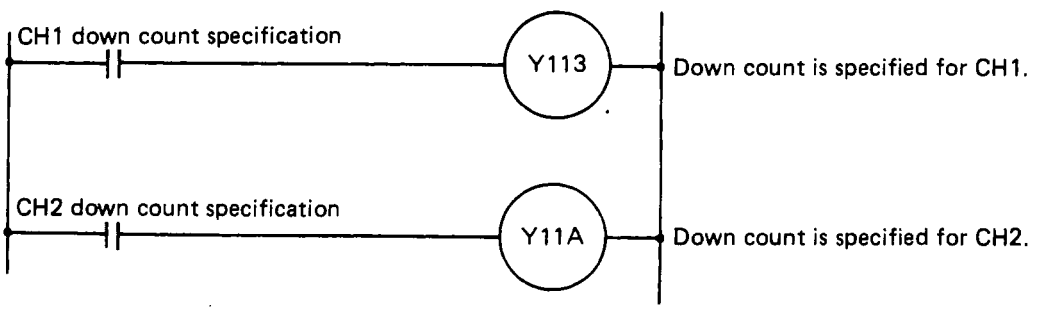
Address of mode register

	Address
CH1	K3
CH2	K35

Data to be written when 2 phases have been specified (in decimal)

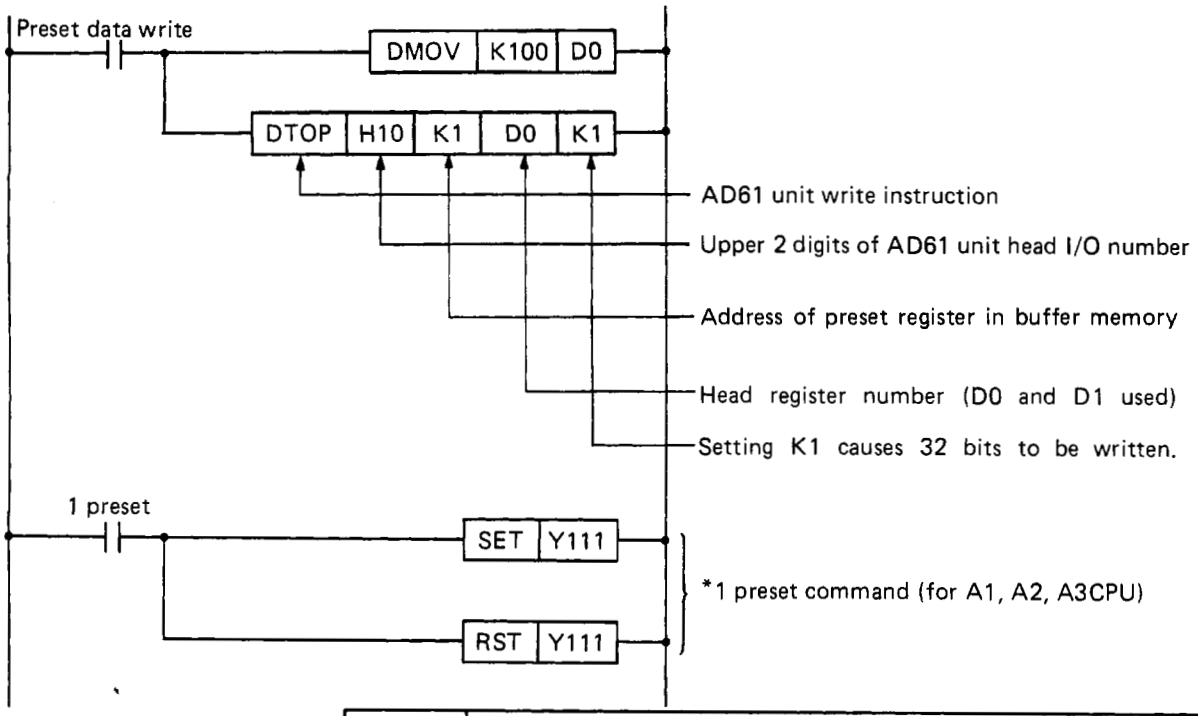
2-phase mode	K18
Word length	K1

(4) Setting of up/down count when 1-phase has been specified.



- When Y113 or Y11A is off, up count is made.
- When the power is turned on or the CPU is reset, both Y113 and Y11A are off.

(5) Setting of preset value data (to set preset value to 100)


Preset data write
DMOV K100 D0
DTOP H10 K1 D0 K1
AD61 unit write instruction
Upper 2 digits of AD61 unit head I/O number
Address of preset register in buffer memory
Head register number (D0 and D1 used)
Setting K1 causes 32 bits to be written.
1 preset
SET Y111
RST Y111
*1 preset command (for A1, A2, A3CPU)

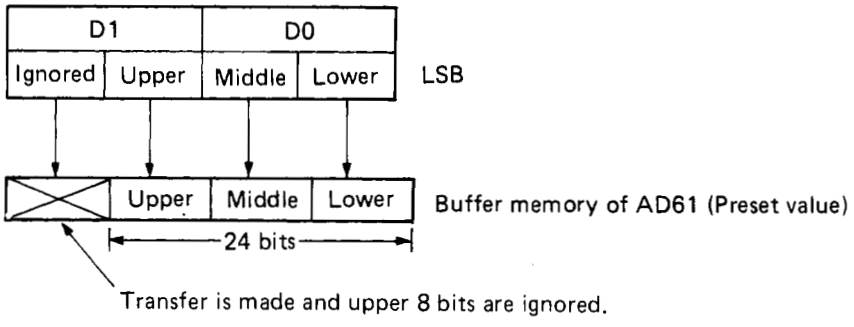
POINT

***1: When using the A1E, A2E, or A3ECPU, use the partial refresh instructions.**

1. Address of preset value

	Address
CH1	K1
CH2	K33
Word length	K1

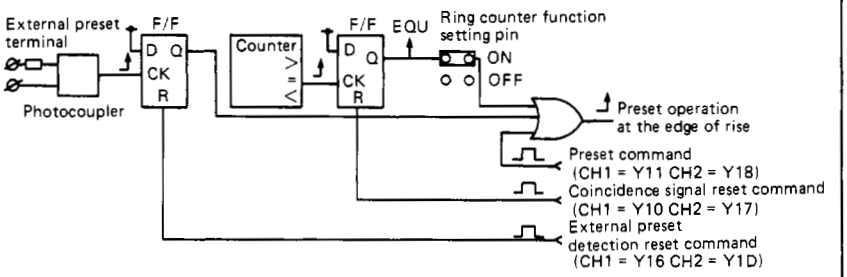
2. Write operation



3. When preset command signal turns on, preset value is set as the initial value of counter at the edge of rise.
   - ○ If external preset request detection signal remains on, preset operation is not performed even when the above instructions are executed. Before turning on preset, it is necessary to execute external preset detection signal reset.
   - ○ After preset value write has been executed, preset can be made at any position.

POINT

A block diagram related to the preset operation of the AD61 is shown below.

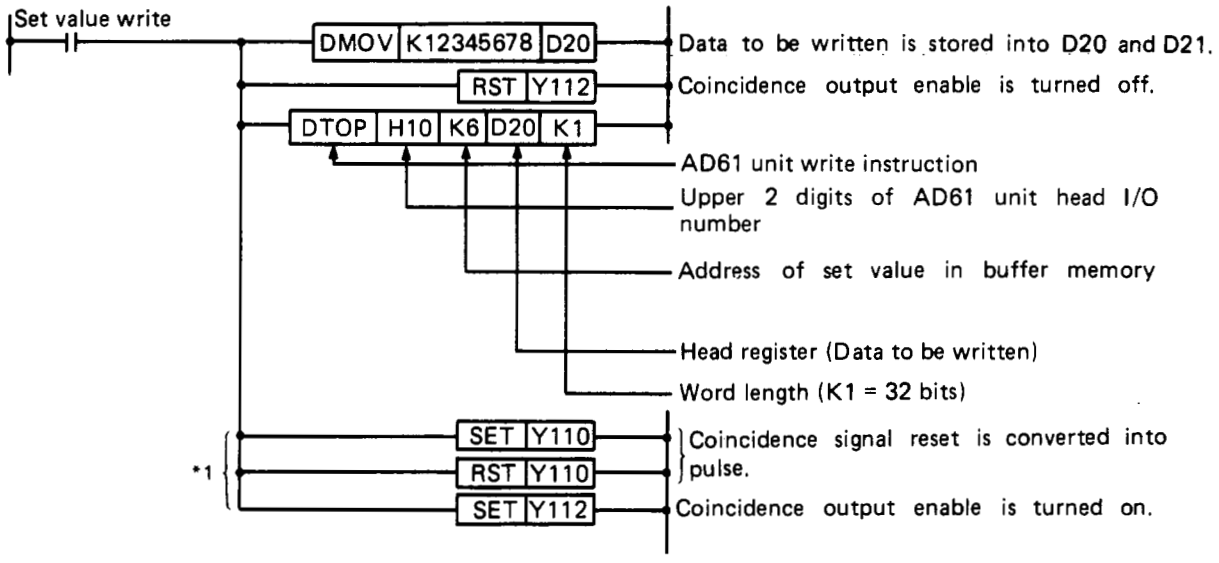


Three signals are available for preset operation.

1. **Preset by program**
2. **Input from external preset terminal**
3. **Counter coincidence when ring counter is on**

Preset operation uses logical add (OR) of these three signals. Upon rise of this signal from off to on, preset operation is performed. If one of the signals remains on, preset operation is not performed because, if another preset signal is turned from off to on, the output of logical add remains on. When ring counter function has been selected, counter value coincidence signal (preset signal) and external preset signal are latched by flip flop. Therefore, it is necessary to provide a reset signal to each of them.

(6) Setting of set value data


Set value write
DMOV K12345678 D20
Data to be written is stored into D20 and D21.
RST Y112
Coincidence output enable is turned off.
DTOP H10 K6 D20 K1
AD61 unit write instruction
Upper 2 digits of AD61 unit head I/O number
Address of set value in buffer memory
Head register (Data to be written)
Word length (K1 = 32 bits)
*1
SET Y110
RST Y110
Coincidence signal reset is converted into pulse.
SET Y112
Coincidence output enable is turned on.

POINT

***1: When using the A1E, A2E, or A3ECPU, use the partial refresh instructions.**

Set value address and signal

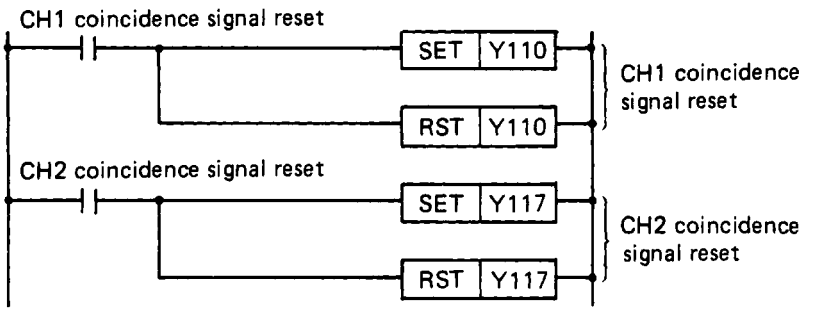
	Address	Coincidence output enable	Coincidence signal reset
CH1	K6	Y112	Y110
CH2	K38	Y119	Y117
Word length	K1		

○When external EQU terminal is not used, RST Y112 and SET Y112 are not required.

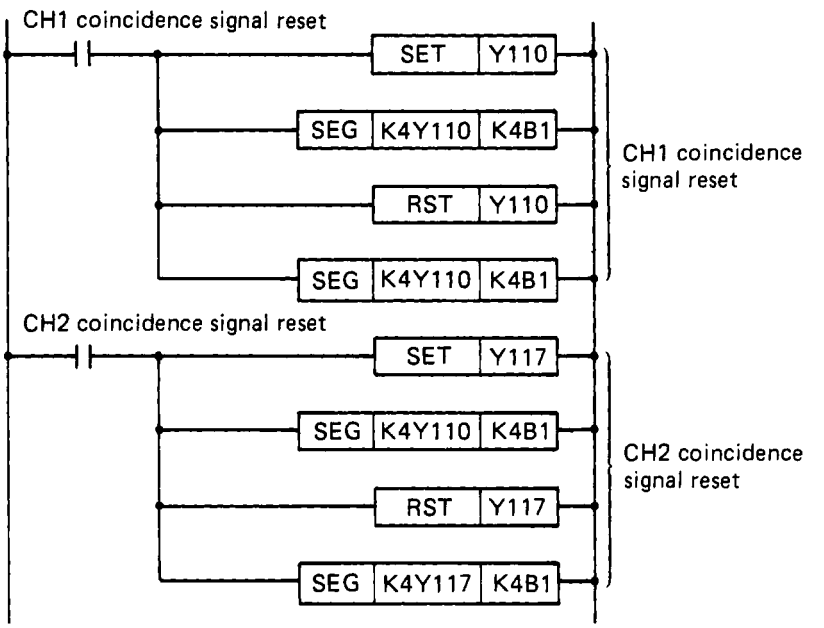
○ When the set value data is written to the buffer memory, the counter value coincidence signal may turn on. For this reason, turn off the coincidence output enable before the set value is written, reset the coincidence signal and finally re-enable the coincidence output.

(7) To reset coincidence signal

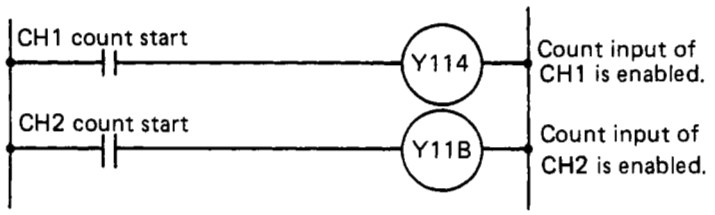
For A1, A2, A3CPU



For A1E, A2E, A3ECPU

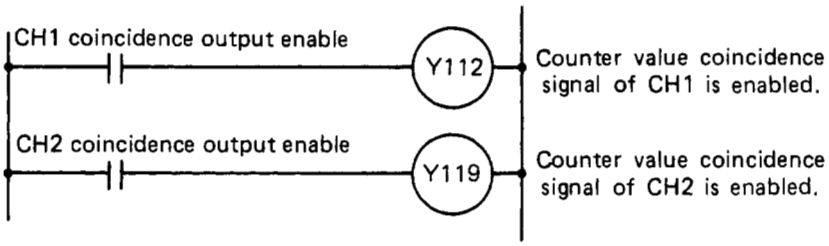


(8) To enable count input



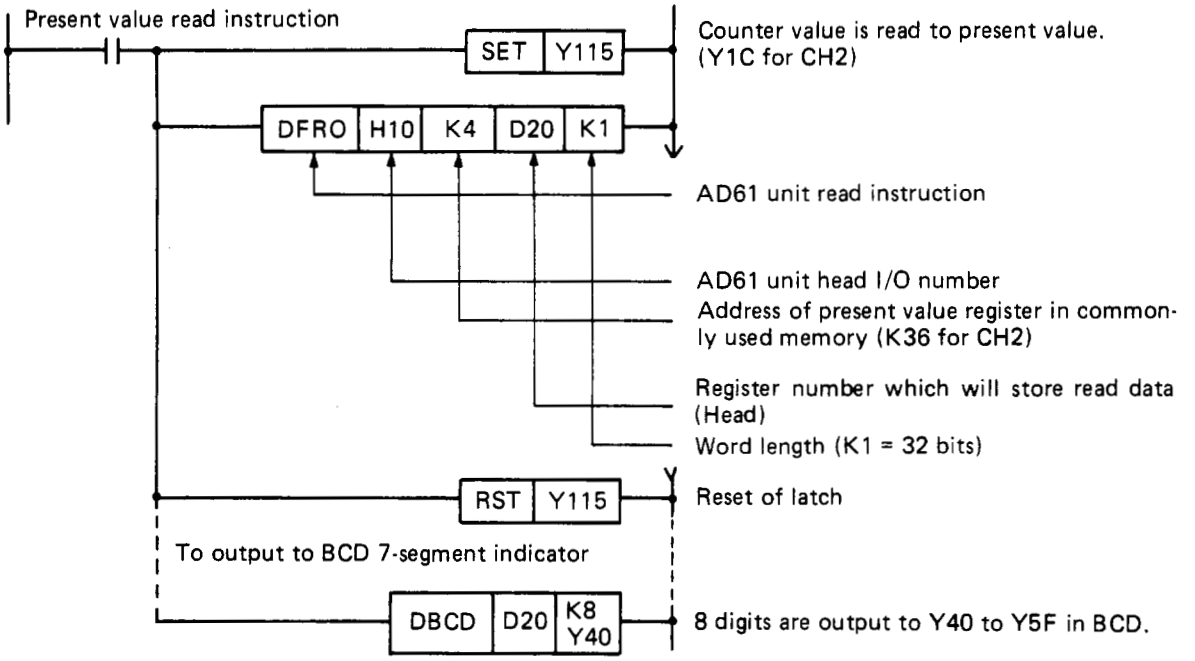
To count signals from the count input terminal block, this signal should be on and the disable input of external terminal block should be off.

(9) To enable coincidence signal output


CH1 coincidence output enable
Y112
Counter value coincidence signal of CH1 is enabled.
CH2 coincidence output enable
Y119
Counter value coincidence signal of CH2 is enabled.

If a counter value is equal to a set value after this signal is turned on, the counter value coincidence signal is output to the EQU terminal. At the same time, "EQU" LED on the indicator at the top of AD61 is lit.

(10) Present value read

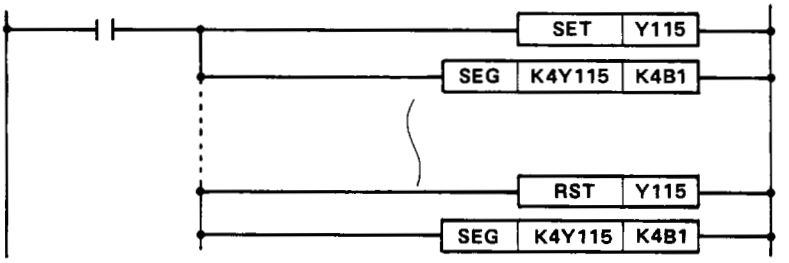

Present value read instruction
SET Y115
Counter value is read to present value. (Y1C for CH2)
DFRO H10 K4 D20 K1
AD61 unit read instruction
AD61 unit head I/O number
Address of present value register in commonly used memory (K36 for CH2)
Register number which will store read data (Head)
Word length (K1 = 32 bits)
RST Y115
Reset of latch
To output to BCD 7-segment indicator
DBCD D20 K8 Y40
8 digits are output to Y40 to Y5F in BCD.

Present value read (decimal)

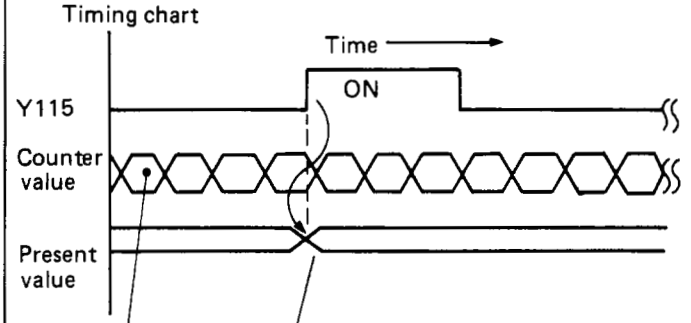
	Address
CH1	K4
CH2	K36
Word length	K1

POINT

When using the A1E, A2E, or A3ECPU, use the partial refresh instructions.



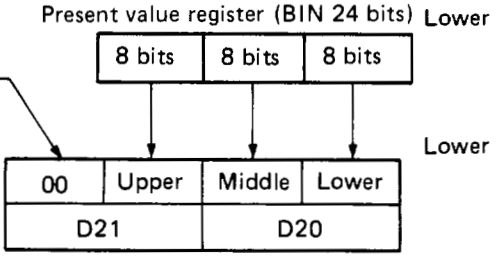
Timing chart



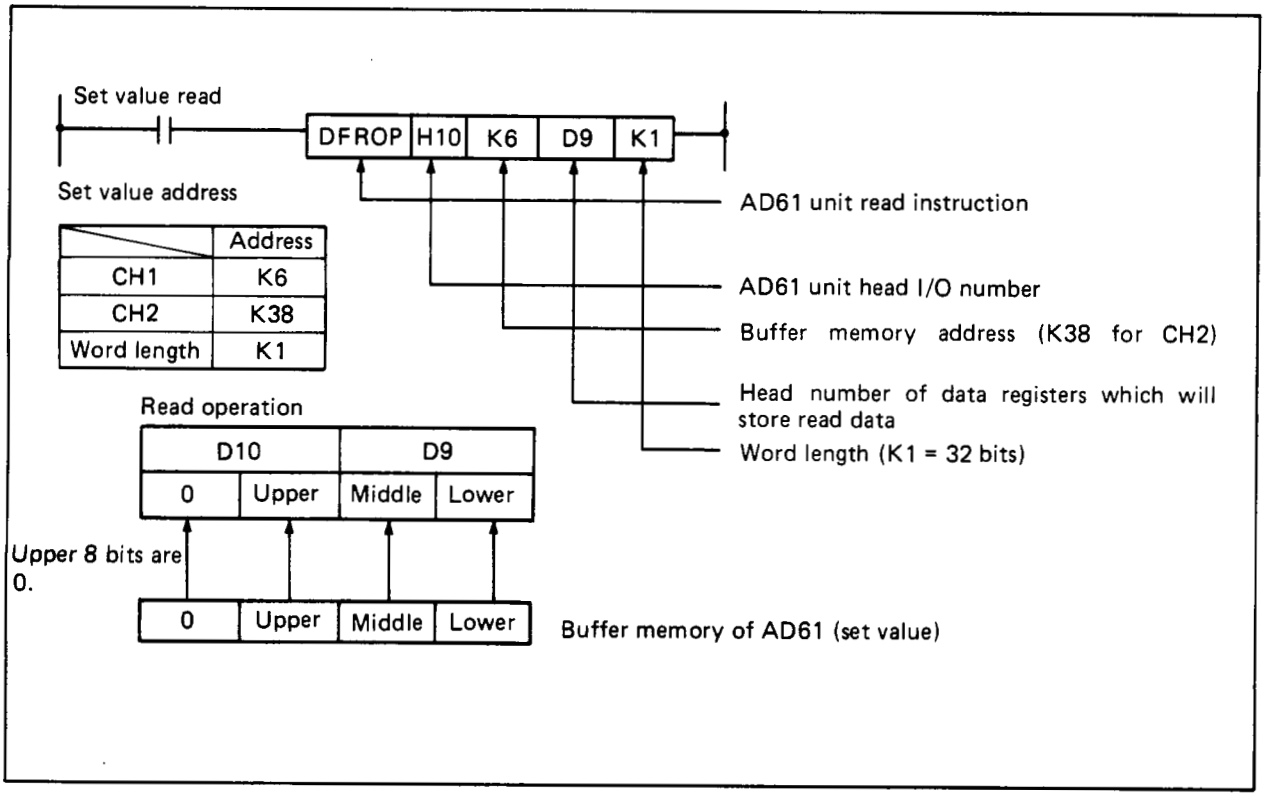
The current value is continuously changing, so to ensure that a correct value is read the above interlock must be used.

Immediately after Y115 turns on, the count value is treated as present value and latched.

At read time, 00 is set into upper 8 bits.

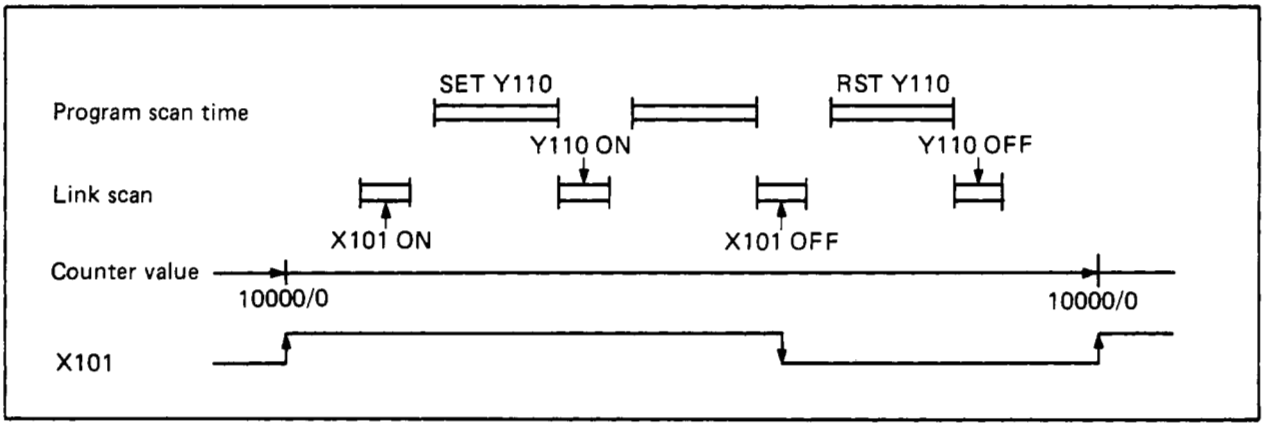


(11) Set value read



6.3 Programming for AD61 in Remote I/O Station

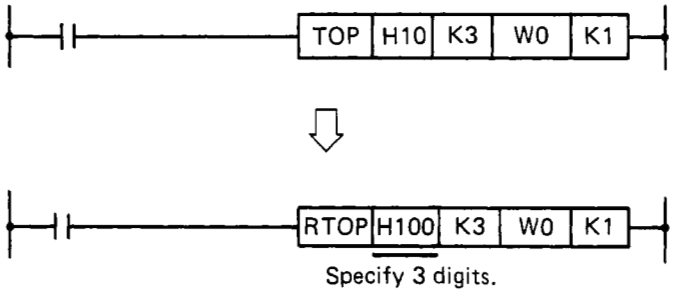
(1) When using the AD61 in a remote I/O station all data and I/O signals must be passed via the link memory. This memory is only accessed after the END command in the main program has been executed so all handshake signals between the AD61 and the CPU will take several scans to be completed.
For example, consider the resetting of the coincidence signals (X01) using the coincidence signal reset command (Y10) (Assume that the AD61 is loaded into the slot corresponding to head number X/Y 100 and the coincidence occurs when the counter current value reaches 10000)



The above example operates correctly because the time taken for the counter to count from 0 to its set value (10000) is greater than the time taken for the handshake signals to operate. If this count time was reduced (i.e. the pulse frequency increased) so that it became less than the time taken to complete the full handshake operation, the AD61 would mis-operate and continue counting above 10000.
It is very important to be aware of this potential problem when using the high speed counter in a remote I/O station. Careful consideration of the main program scan time, the link scan time and the pulse frequency will avoid mis-operation, however it is recommended that the AD61 is used only in stations with their own CPU. If the AD61 is used in a remote I/O station, the handshake sequences described in this section should be used with caution.

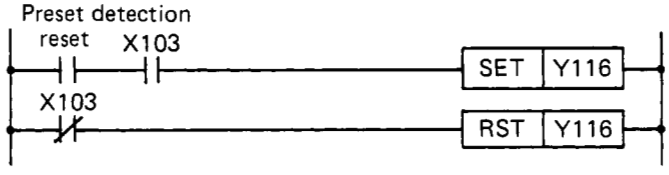
(2) For the communication program to and from the remote I/O station, use RTOP to write to the AD61 and RFRP to read from the AD61.
The RTOP and RFRP instructions differ from TO and FROM in the following point: To set the AD61 head I/O numbers, specify upper 2 digits for TO and FROM. Specify all digits for RTOP and RFRP. (Refer to the Data Link Unit User's Manual.)

Example: AD61 head I/O numbers assigned to X/Y100 to X/Y11F.

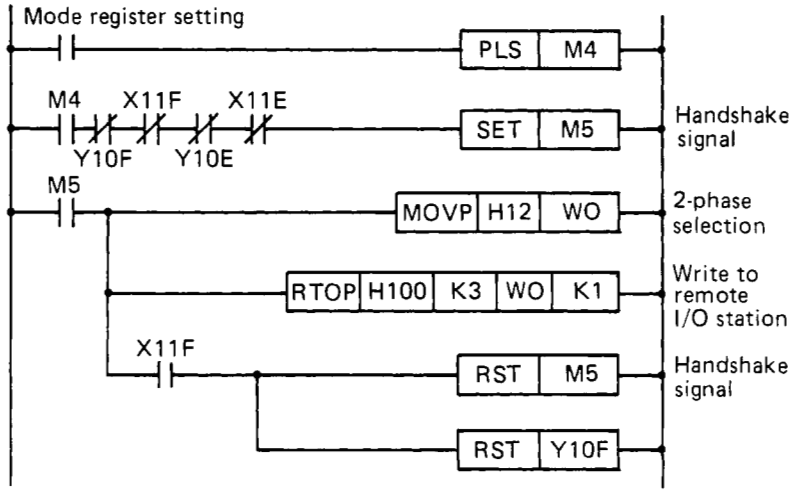


All data is communicated via the link registers. The link registers W should be set in the programmable controller CPU parameters. In the following example, the AD61 is assigned to X/Y100 to X/Y11F.

○ External preset detection reset



○ Mode register setting



7. TEST OPERATION

7.1 Pre-test Checks

IMPORTANT

Before switching on the encoder power supply, check that the correct terminals have been used. Application of 24V to 5V terminals will damage the unit.

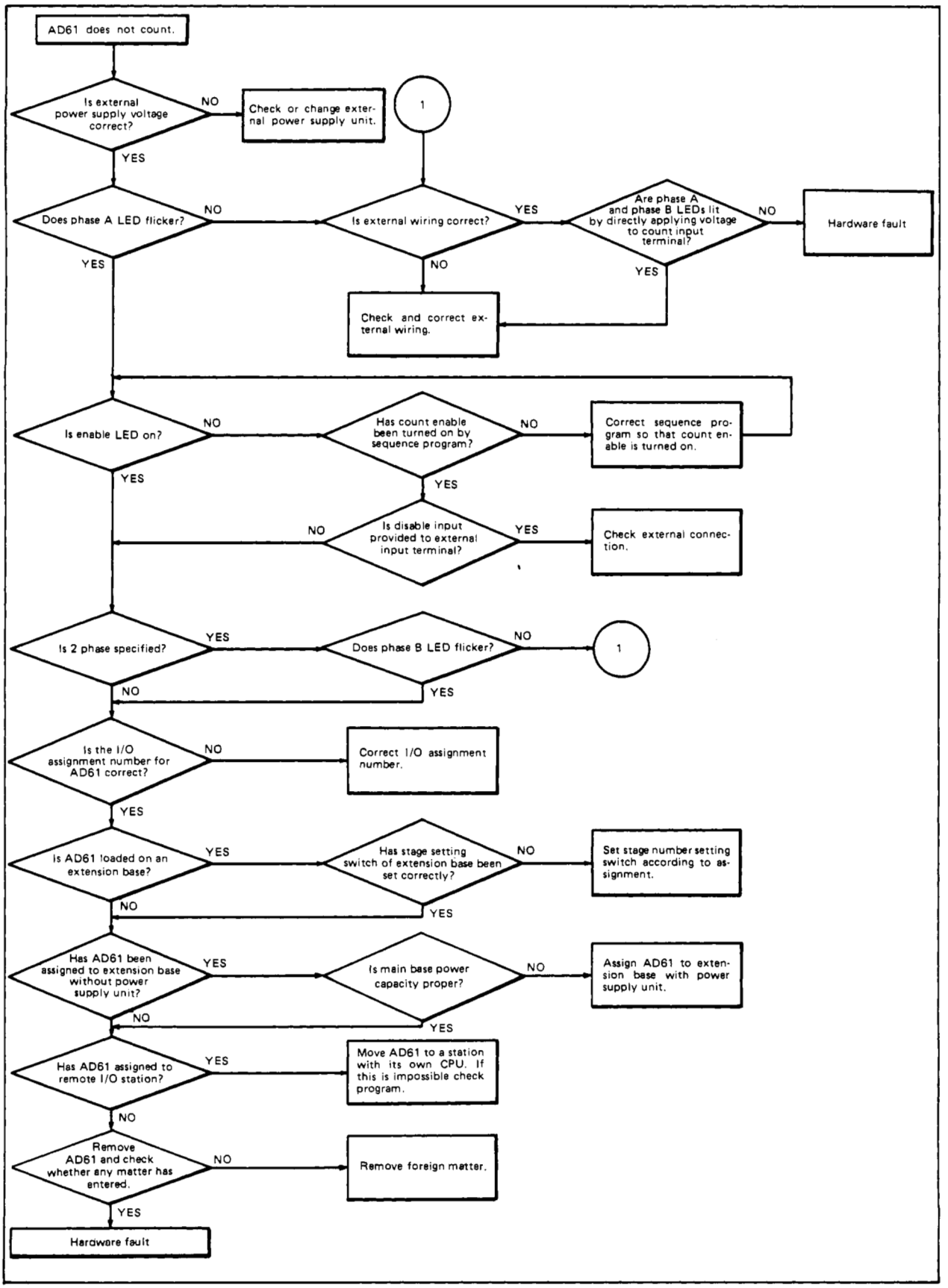
Before turning on the power, check the following:

1. Ring counter setting pin.
2. Check that the AD61 is properly loaded onto the base unit.
3. Check terminal wiring.
4. Check the voltage of the external power supply.

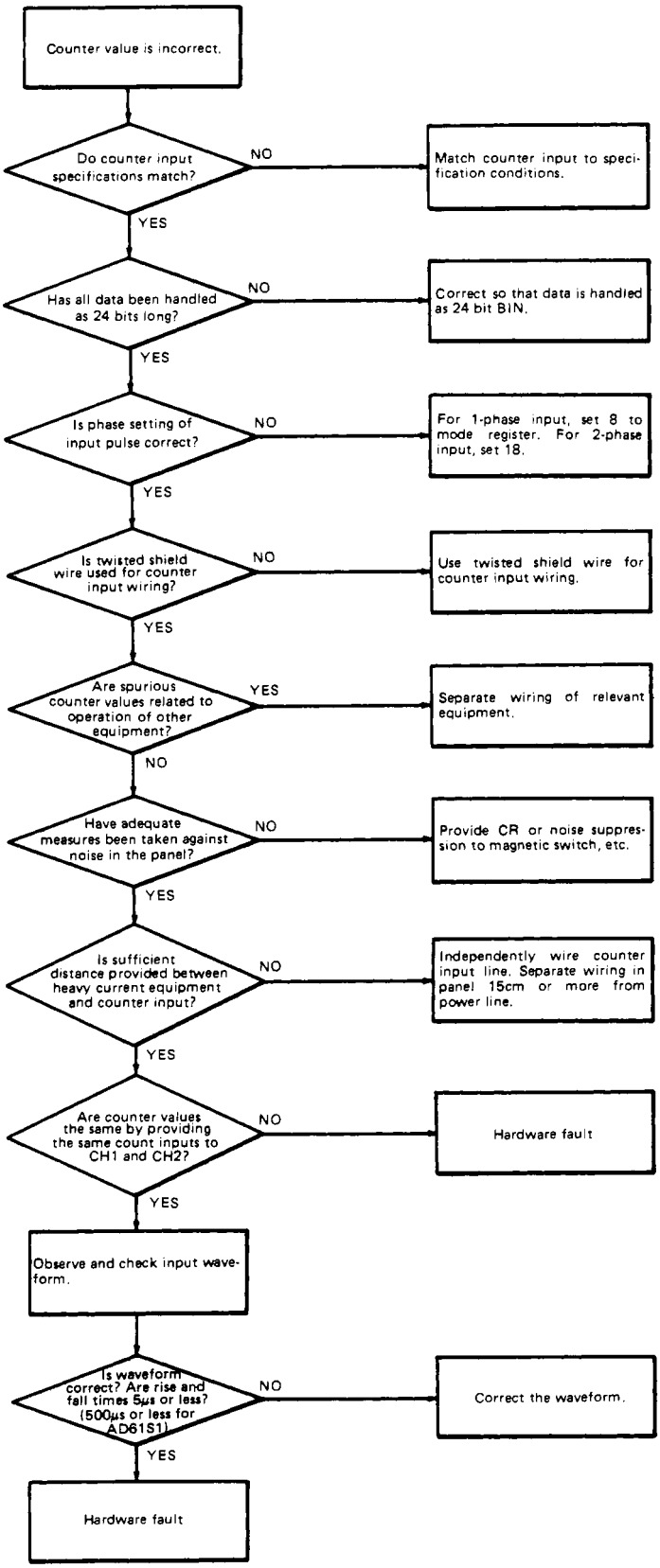
After the above checks, turn on the power and operate the pulse generator. Check the relevant phase indicator LED.

8. TROUBLESHOOTING

AD61 does not count.



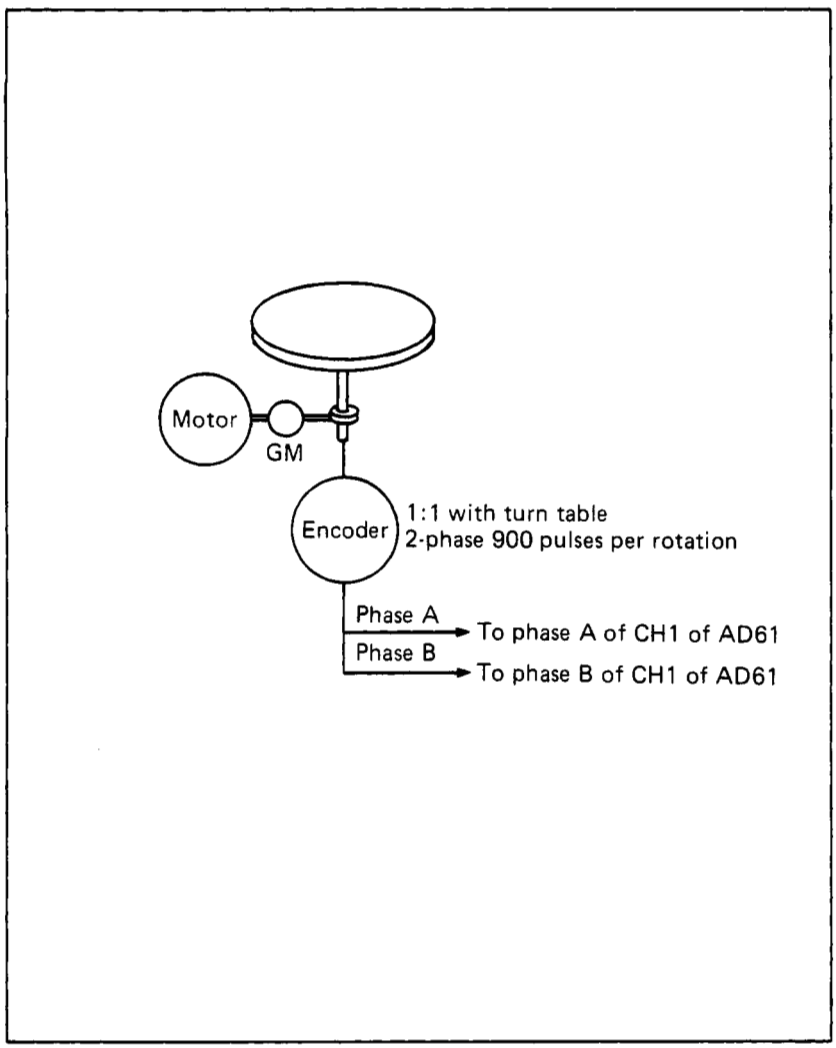
Counter value is incorrect.


Counter value is incorrect.
Do counter input specifications match?
NO
Match counter input to specification conditions.
YES
Has all data been handled as 24 bits long?
NO
Correct so that data is handled as 24 bit BIN.
YES
Is phase setting of input pulse correct?
NO
For 1-phase input, set 8 to mode register. For 2-phase input, set 18.
YES
Is twisted shield wire used for counter input wiring?
NO
Use twisted shield wire for counter input wiring.
YES
Are spurious counter values related to operation of other equipment?
YES
Separate wiring of relevant equipment.
NO
Have adequate measures been taken against noise in the panel?
NO
Provide CR or noise suppression to magnetic switch, etc.
YES
Is sufficient distance provided between heavy current equipment and counter input?
NO
Independently wire counter input line. Separate wiring in panel 15cm or more from power line.
YES
Are counter values the same by providing the same count inputs to CH1 and CH2?
NO
Hardware fault
YES
Observe and check input waveform.
Is waveform correct? Are rise and fall times 5μs or less? (500μs or less for AD61S1)
NO
Correct the waveform.
YES
Hardware fault

APPENDICES

APPENDIX 1 Application Circuit Examples

(1) Example of turn table indexing



Operation

The indexing table is positioned at a corresponding to the digital switch setting (0 to 3599). The encoder is directly connected to the turn table rotating shaft. The encoder gives 900 pulses per rotation, 2-phase.

I/O assignment

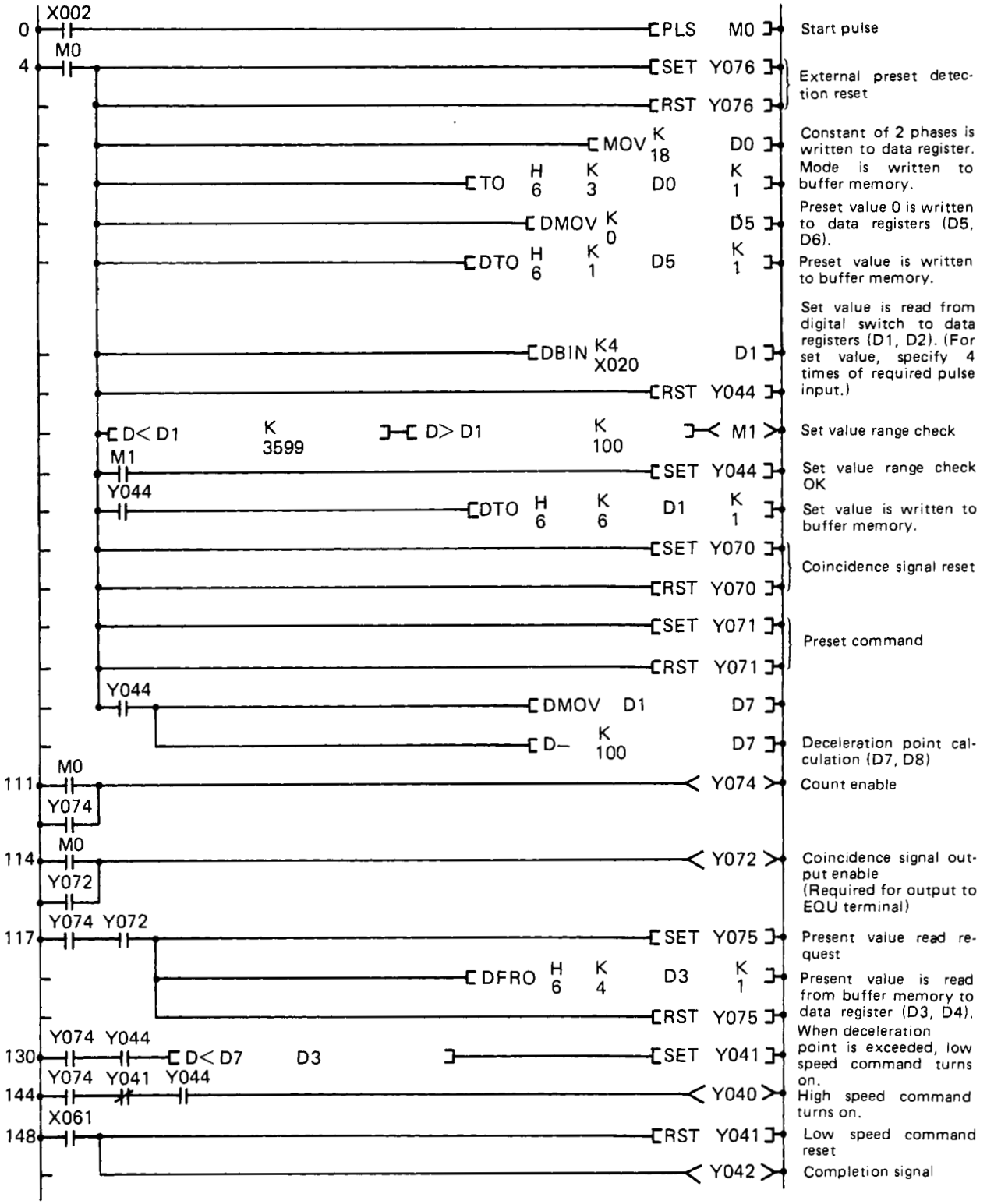
X60 to X6F Y70 to Y7F	AD61
X20 to X2F	4 digits of digital switch
X02	Start switch
Y40	Motor high speed
Y41	Motor low speed
Y42	Completion signal
Y44	Set value range OK

Data register assignment

D0	Mode
D1, D2	Set value
D3, D4	Present value
D5, D6	Preset value
D7, D8	Deceleration point value

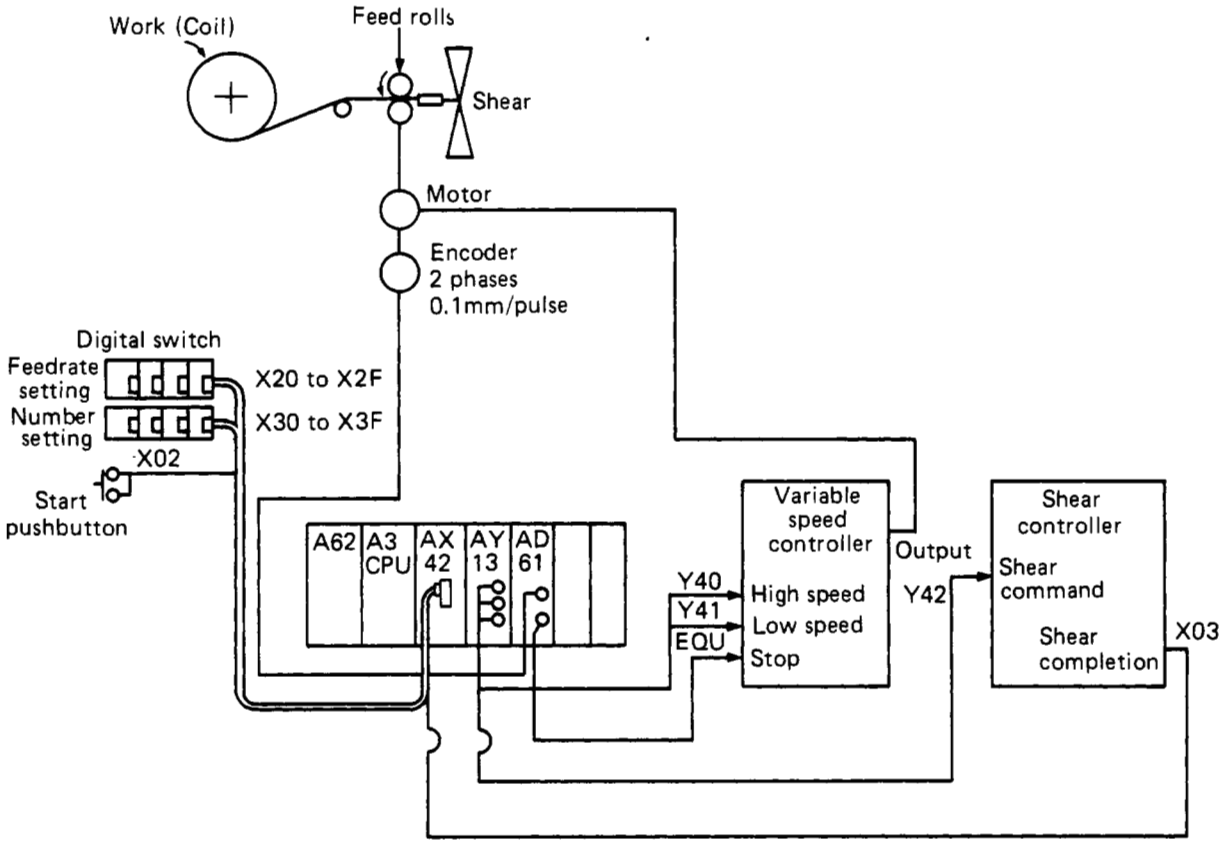
When the start pushbutton is pressed, the motor rotates at high speed and present the value is read. 10 degrees ahead of the indexing point, the speed is reduced. When the counter value coincidence signal turns on, the turn table is brought to a stop. (If the set value is 10 degrees (100 counts) or less, the program does not operate.)

Example of turn table indexing



(2) Example using ring counter function

Shearing control application using the ring counter functio



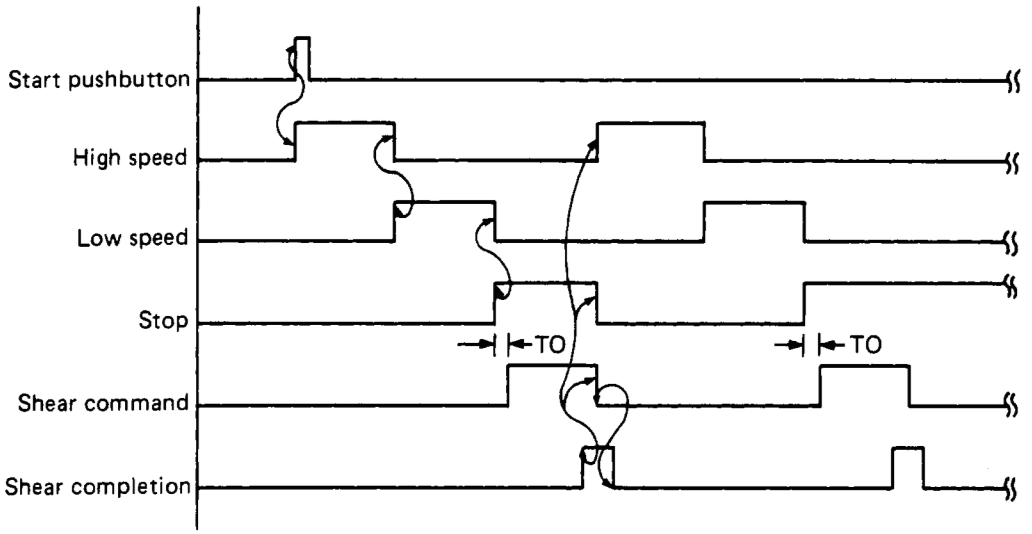
Operation

When the start pushbutton is pressed, the amount set by the feedrate digital switch is advanced. When positioning is completed, a shear command is sent to the shear controller. When shearing is complete, the positioning operation is repeated. (Deceleration point is 100 counts ahead of the set value. If the set value is 100 counts or less, the program does not operate.)

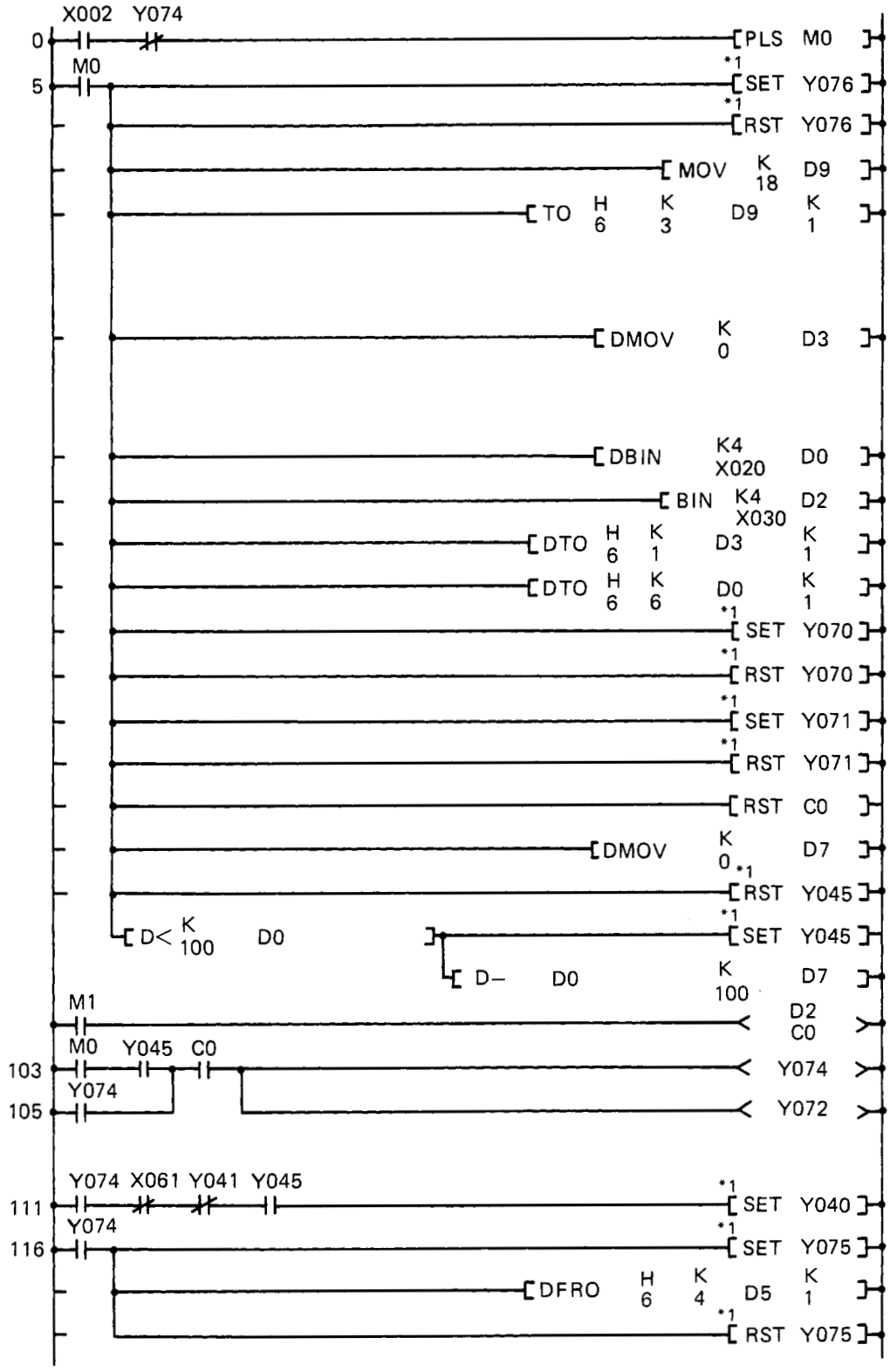
Data register assignment

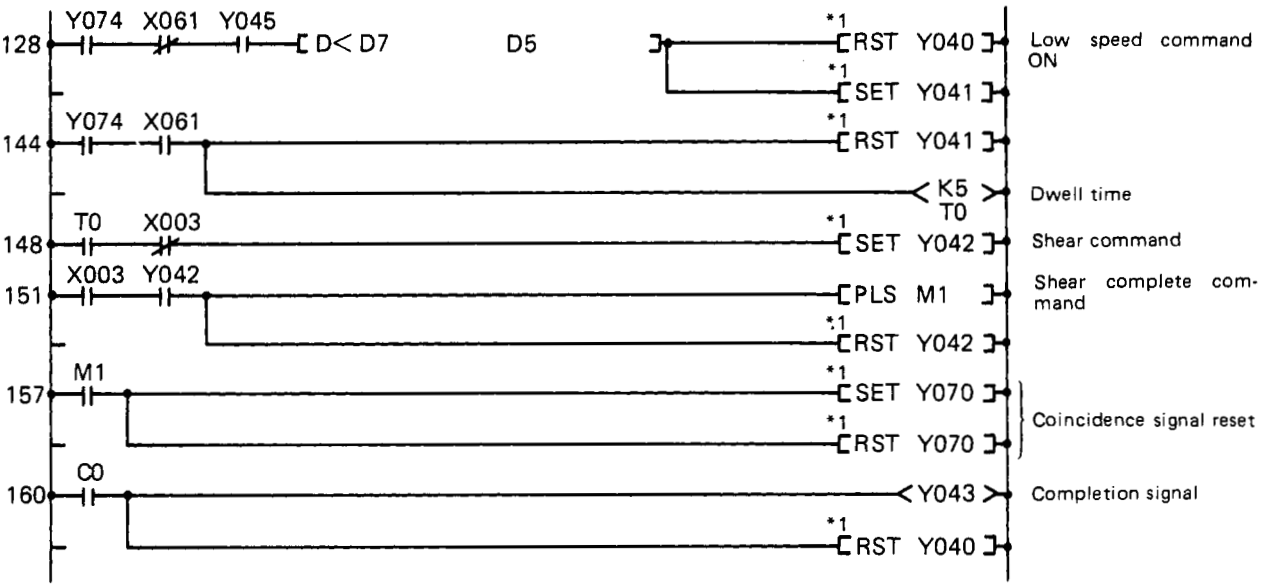
D0, D1	Set value
D2	Number value
D3, D4	Preset value
D5, D6	Present value

Operation timing
(Number setting = 2)



Application circuit using ring counter function (for A1, A2, A3CPU)


X002 Y074
0
PLS M0
Start pulse
M0
5
*1 SET Y076
*1 RST Y076
External preset detection reset
MOV K 18 D9
Constant of 2 phases is written to data register.
TO H 6 K 3 D9 K 1
Mode is written to buffer memory.
Preset value 0 is written to data registers (D3, D4).
DMOV K 0 D3
Set value is read from digital switch to data registers (D1, D2). (For set value, specify 4 times of required pulse input.)
DBIN K4 X020 D0
BIN K4 X030 D2
Number value is read from digital switch.
DTO H 6 K 1 D3 K 1
Preset value is written to buffer memory.
DTO H 6 K 6 D0 K 1
Set value is written to buffer memory.
*1 SET Y070
*1 RST Y070
Coincidence signal reset
*1 SET Y071
*1 RST Y071
Preset command
RST C0
Number counter reset
DMOV K 0 D7
Deceleration point clear
*1 RST Y045
D< K 100 D0
*1 SET Y045
Set value range check OK
D– D0 K 100 D7
Calculation of deceleration point (D7, D8)
M1
D2 C0
M0 Y045 C0
103
Y074
Count enable
Y074
105
Y072
Coincidence signal output enable (Required for output to EQU terminal)
Y074 X061 Y041 Y045
111
*1 SET Y040
High speed command ON
Y074
116
*1 SET Y075
Present value read request
DFRO H 6 K 4 D5 K 1
Present value is read from buffer memory to data registers (D5, D6).
*1 RST Y075

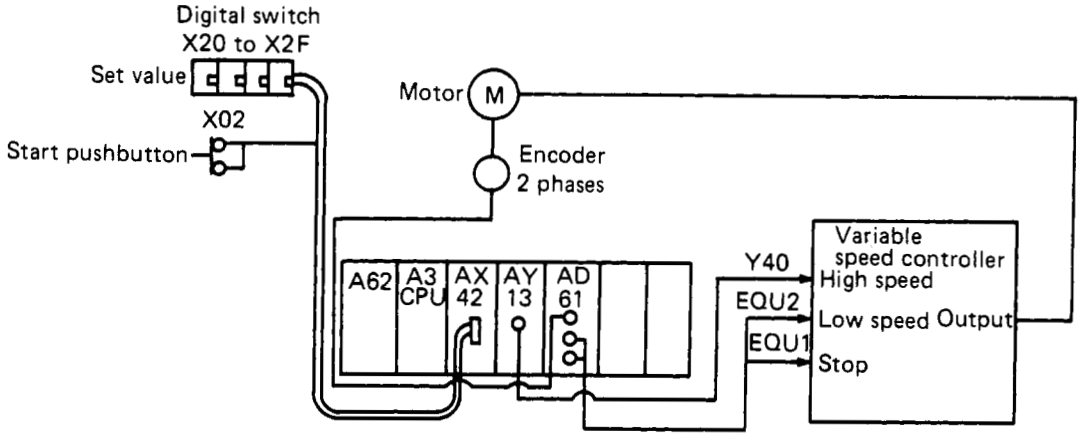


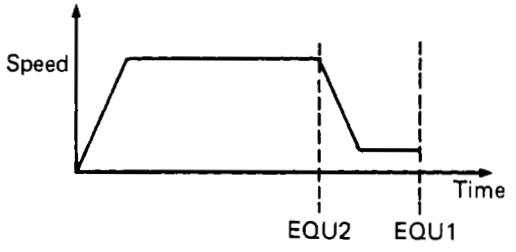
POINT

When using the A1E, A2E, or A3ECPU, use the partial refresh instructions at places marked * in the program.

(3) Example using CH1 and CH2 coincidence signal output

This section shows a high-speed response positioning circuit example which uses the coincidence signal outputs of CH1 and CH2 (EQU1 and EQU2) and has no relation to the scan time of the sequence program.



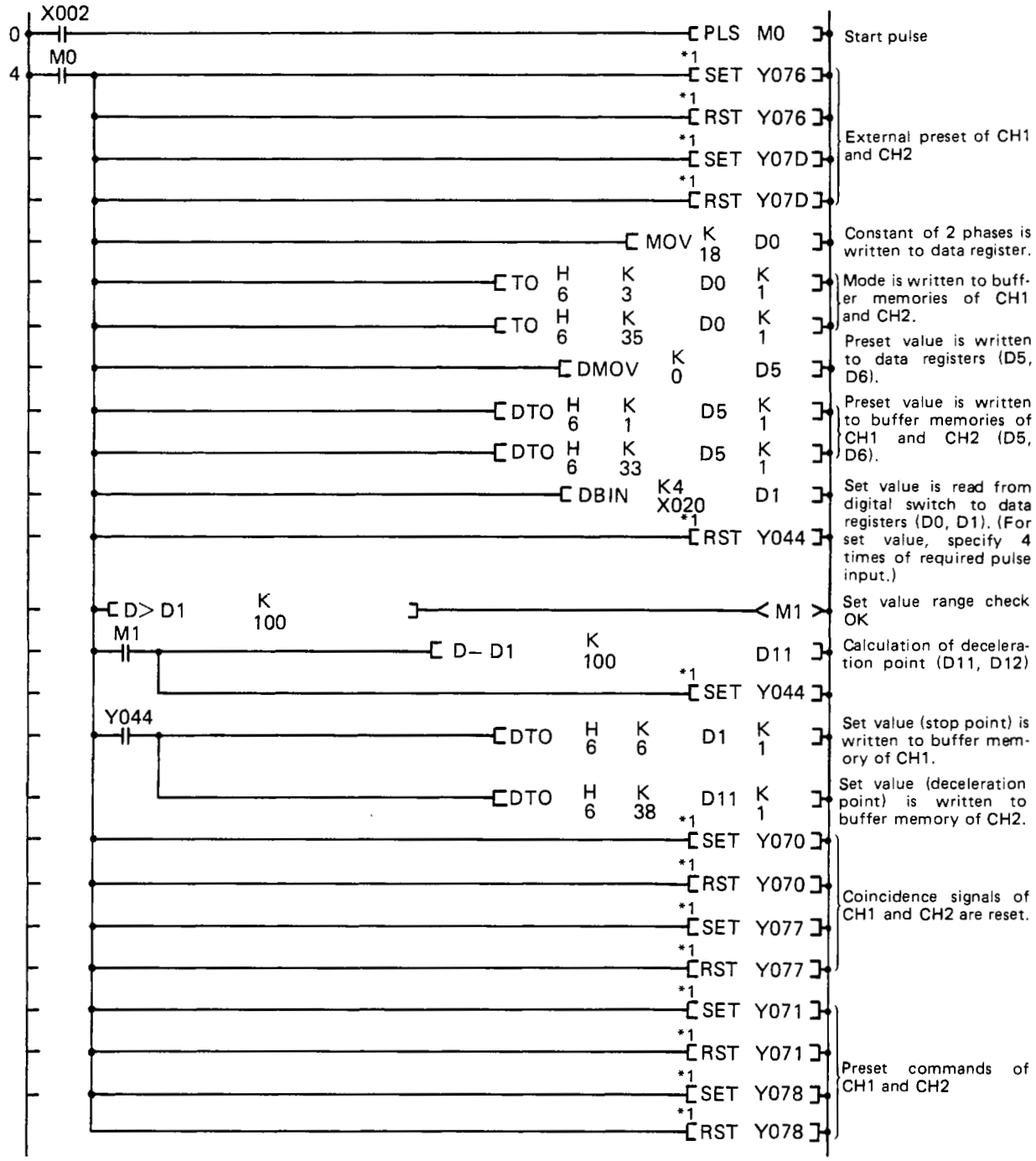


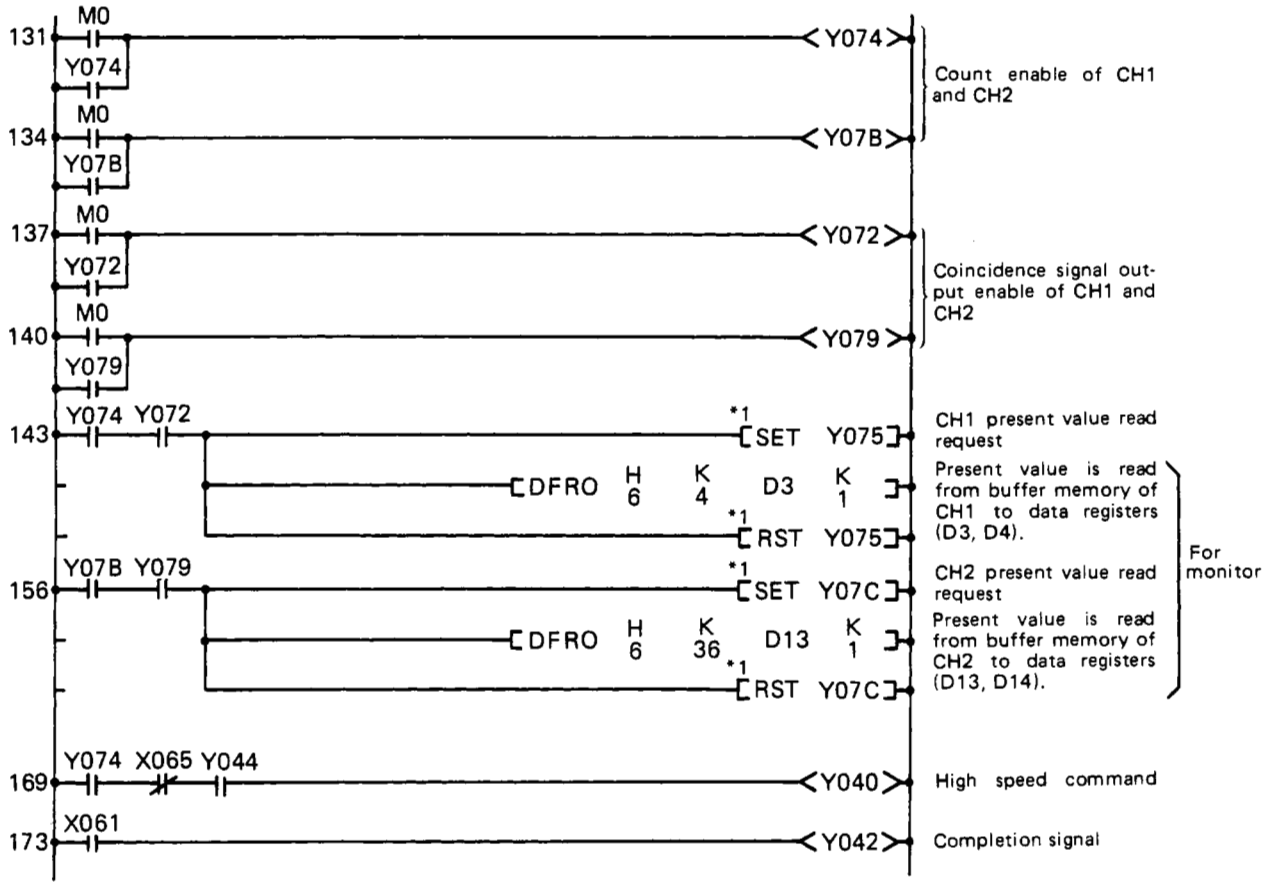
Operation

When the start pushbutton is pressed, the set value is read from the digital switch, output Y is provided, and positions the job at high-speed, using the output signals EQU1 and EQU2.
(Deceleration point is 100 counts ahead of set value. If the set value is 100 counts or less, program does not operate.)

Data register assignment

D0	Modes of CH1 and CH2
D1, D2	Set value of CH1
D3, D4	Present value of CH1
D5, D6	Preset values of CH1 and CH2
D11, D12	Set value of CH2
D13, D14	Present value of CH2

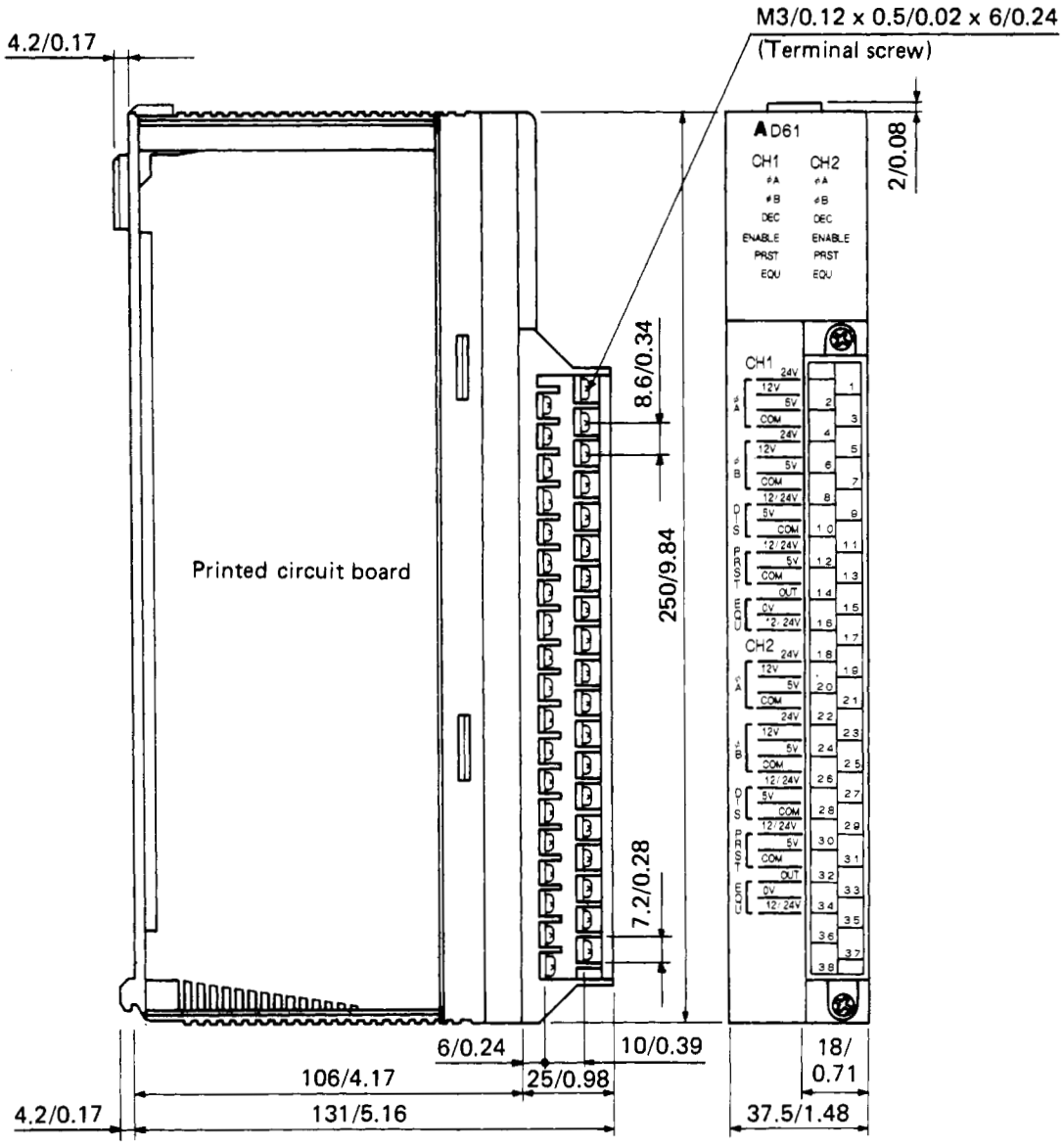

X002
0
PLS M0
Start pulse
M0
4
*1 SET Y076
*1 RST Y076
*1 SET Y07D
*1 RST Y07D
External preset of CH1 and CH2
MOV K 18 D0
Constant of 2 phases is written to data register.
TO H 6 K 3 D0 K 1
TO H 6 K 35 D0 K 1
Mode is written to buffer memories of CH1 and CH2.
DMOV K 0 D5
Preset value is written to data registers (D5, D6).
DTO H 6 K 1 D5 K 1
DTO H 6 K 33 D5 K 1
Preset value is written to buffer memories of CH1 and CH2 (D5, D6).
DBIN K4 X020 D1
*1 RST Y044
Set value is read from digital switch to data registers (D0, D1). (For set value, specify 4 times of required pulse input.)
D> D1 K 100
M1
Set value range check OK
M1
D- D1 K 100 D11
*1 SET Y044
Calculation of deceleration point (D11, D12)
Y044
DTO H 6 K 6 D1 K 1
Set value (stop point) is written to buffer memory of CH1.
DTO H 6 K 38 D11 K 1
Set value (deceleration point) is written to buffer memory of CH2.
*1 SET Y070
*1 RST Y070
*1 SET Y077
*1 RST Y077
Coincidence signals of CH1 and CH2 are reset.
*1 SET Y071
*1 RST Y071
*1 SET Y078
*1 RST Y078
Preset commands of CH1 and CH2



POINT

When using the A1E, A2E, or A3ECPU, use the partial refresh instructions at places marked * in the program.

APPENDIX 2 External View



Unit: mm/inch

IMPORTANT

The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly. If it is necessary to handle them take the following precautions.

(1) Ground human body and work bench.

(2) Do not touch the conductive areas of the printed circuit board and its electrical parts with any non-grounded tools etc.

Under no circumstances will Mitsubishi Electric be liable or responsible for any consequential damage that may arise as a result of the installation or use of this equipment.

All examples and diagrams shown in this manual are intended only as an aid to understanding the text, not to guarantee operation. Mitsubishi Electric will accept no responsibility for actual use of the product based on these illustrative examples.

Owing to the very great variety in possible applications of this equipment, you must satisty yourself as to its suitability for your specific application.

NOTES

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Industrial Automation Division

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